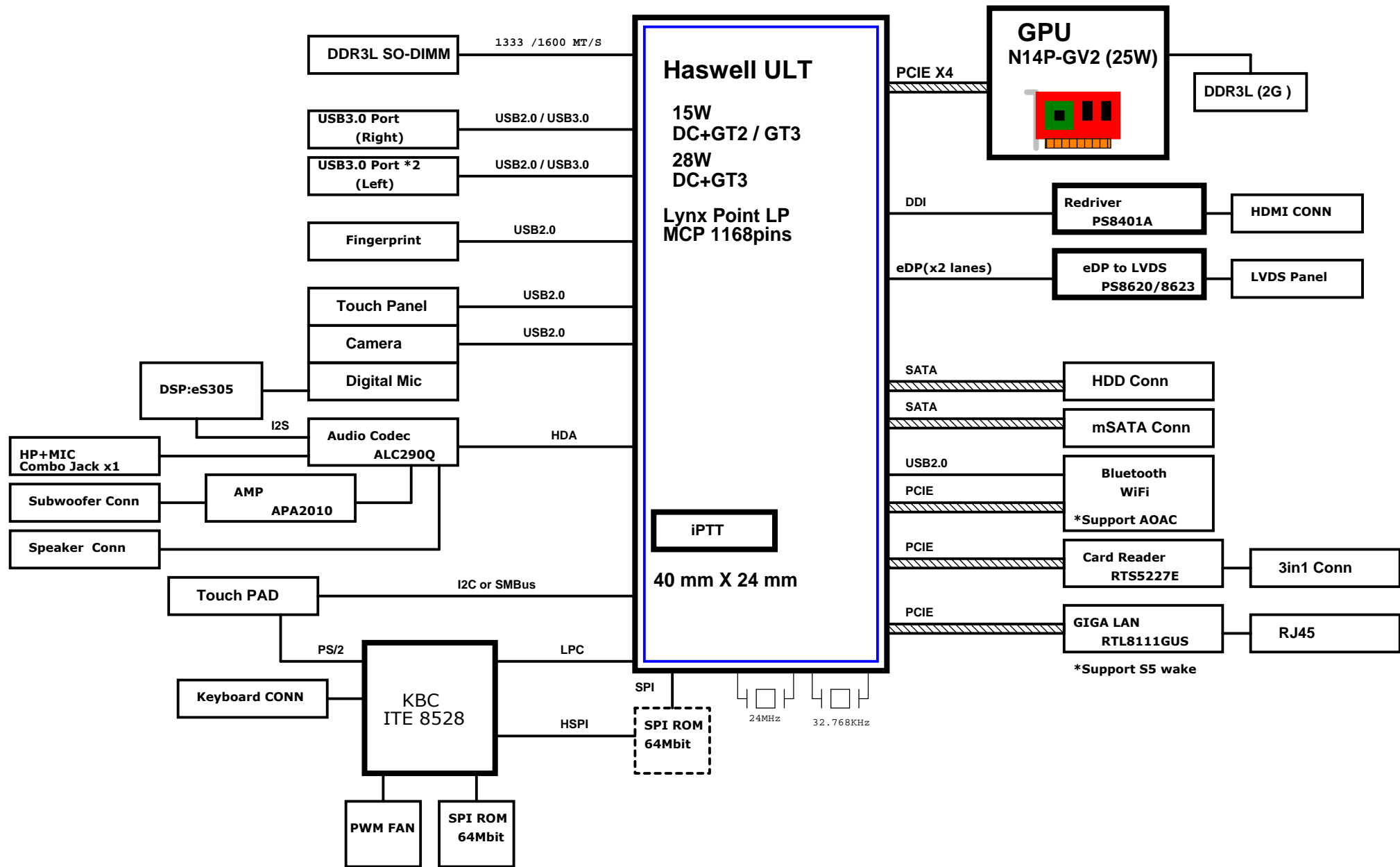


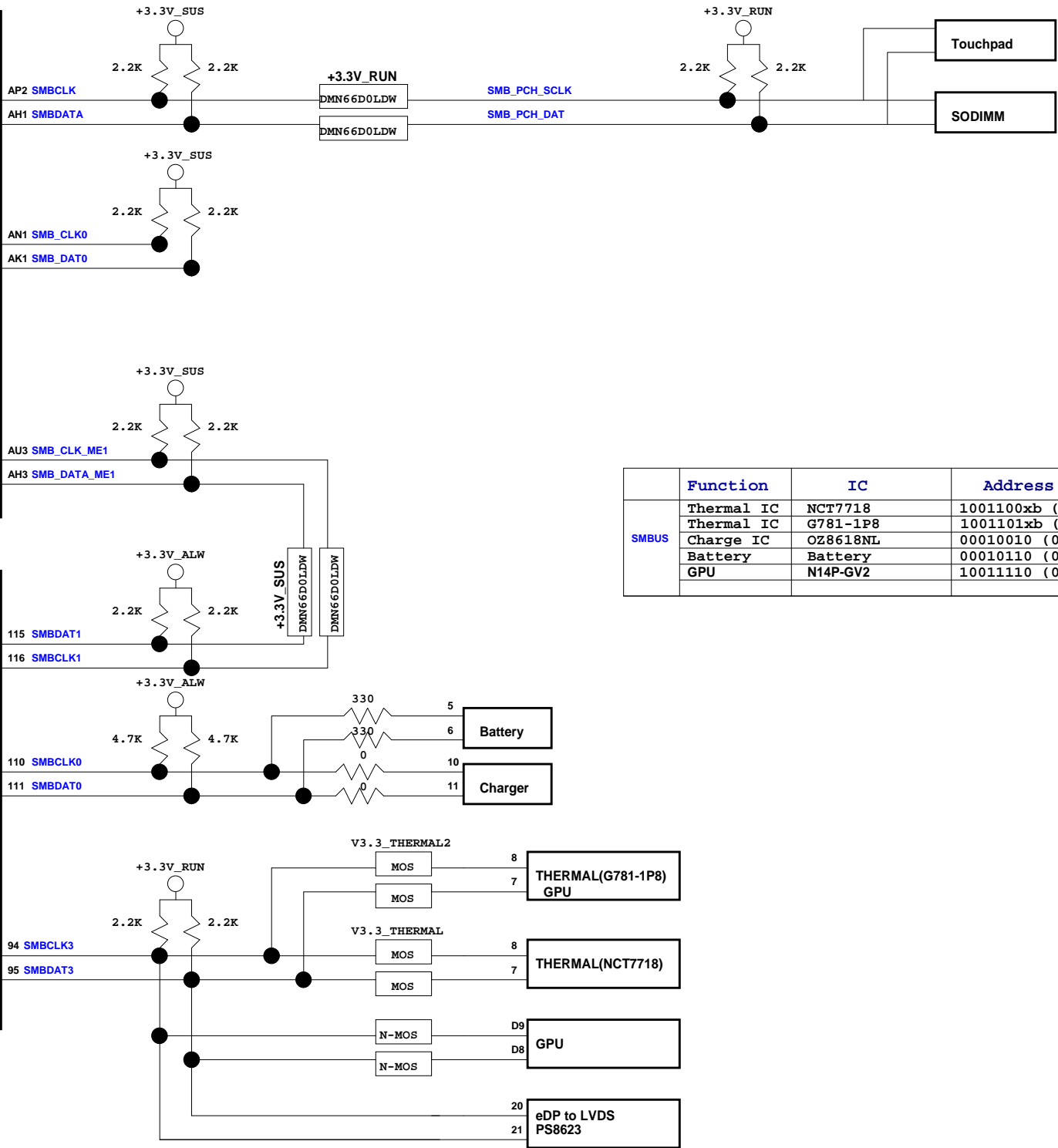
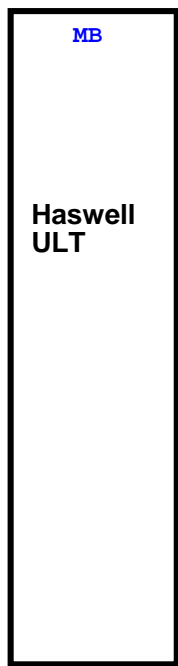
JW8B/C BLOCK DIAGRAM



HSIO Port	USB3.0	PCIE	SATA
1	USB3.0_1 CN6		
2	USB3.0_2 CN4		
3	USB3.0_3 CN5	PCIE1 X	
4	USB3.0_4 X	PCIE2 Card Reader	
5		PCIE3 GIGA LAN	
6		PCIE4 WIFI	
7		PCIE5 GPU 4X	
8		PCIE5 GPU 4X	
9		PCIE5 GPU 4X	
10		PCIE5 GPU 4X	
11		PCIE6 X	SATA3 X
12		PCIE6 X	SATA2 mSATA
13		PCIE6 X	SATA1 HDD
14		PCIE6 X	SATA0 X

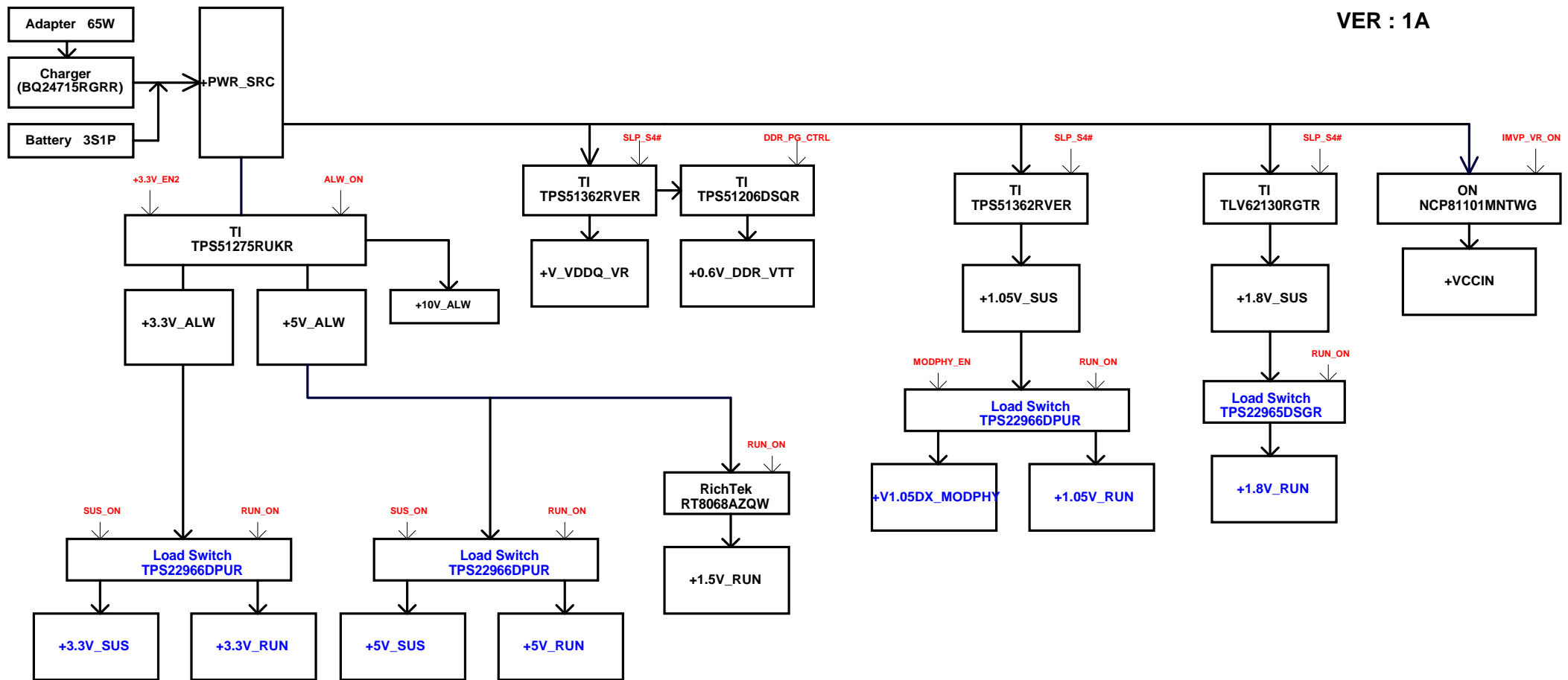
PCIE CLK
CLK0 X
CLK1 Card Reader
CLK2 GIGA LAN
CLK3 WIFI
CLK4 GPU 4X
CLK5 X

USB2.0
USB2.0_0 CN4
USB2.0_1 CN6
USB2.0_2 CN5
USB2.0_3 Finger Print
USB2.0_4 Camera
USB2.0_5 eTP
USB2.0_6 Blue Tooth
USB2.0_7 Touch Screen

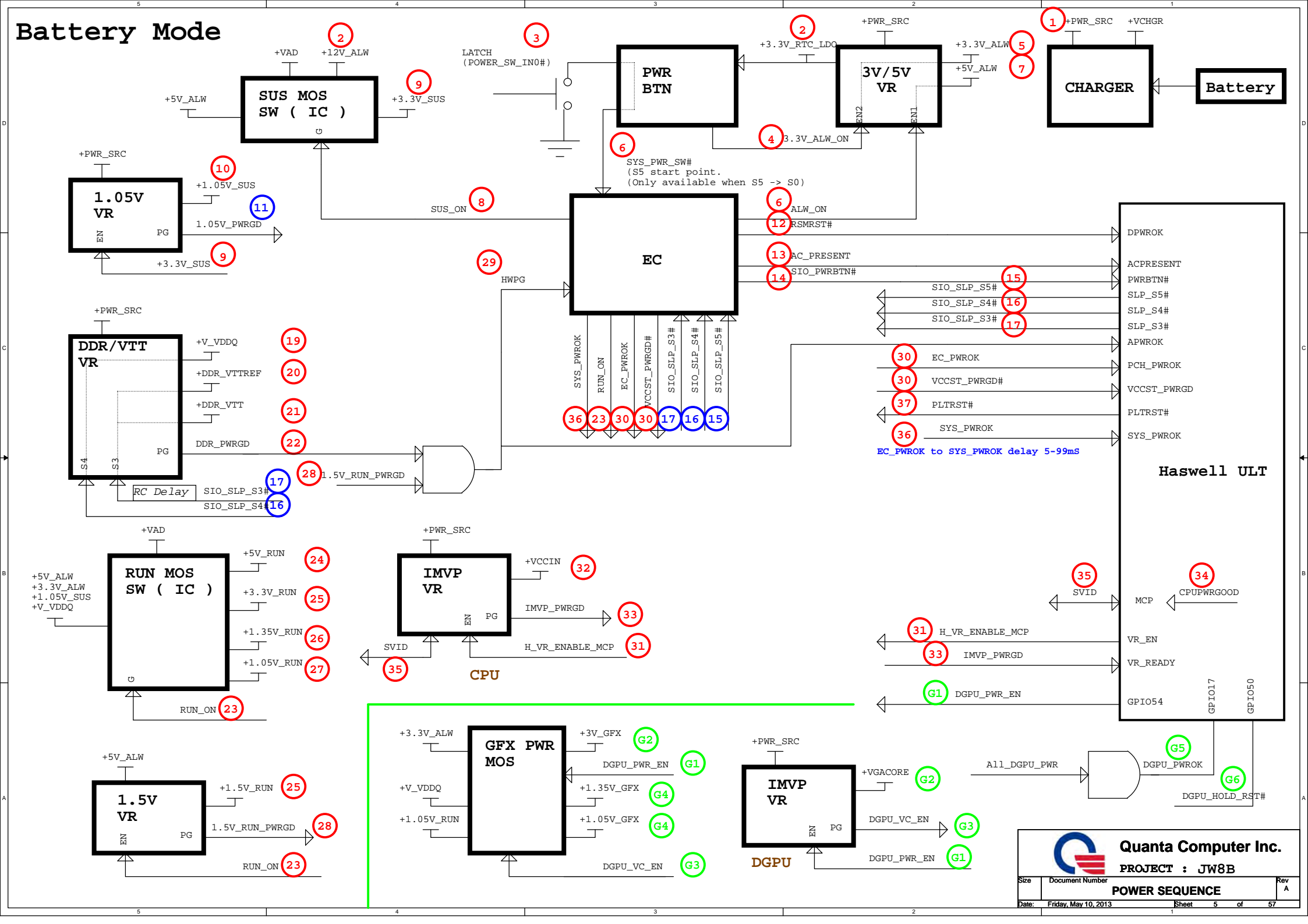


	Function	IC	Address
SMBUS	Thermal IC	NCT7718	1001100xb (98h)
	Thermal IC	G781-1P8	1001101xb (9Ah)
	Charge IC	OZ8618NL	00010010 (0x12h)
	Battery	Battery	00010110 (0X16h)
	GPU	N14P-GV2	10011110 (0X9Eh)

VER : 1A

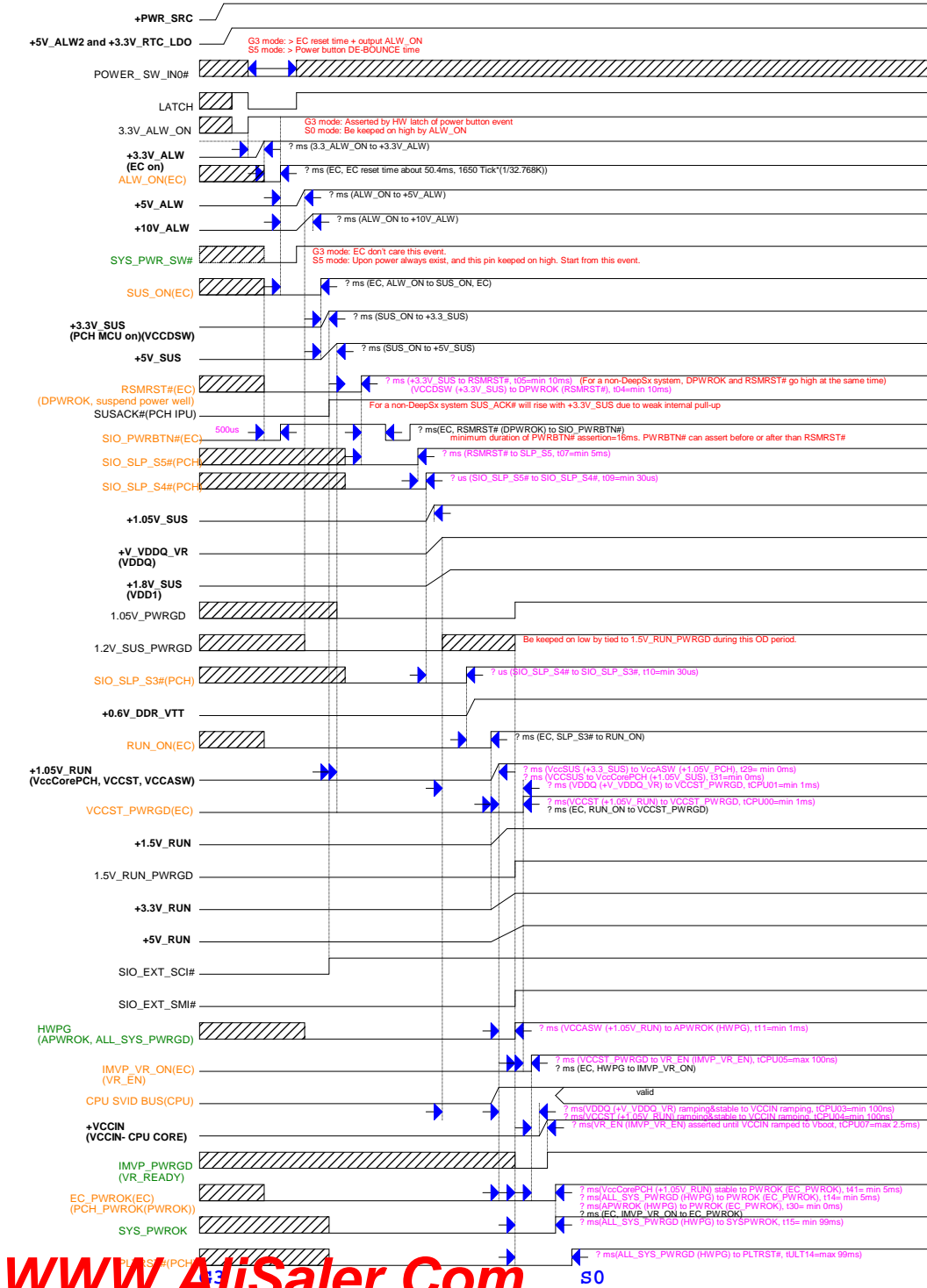


Battery Mode



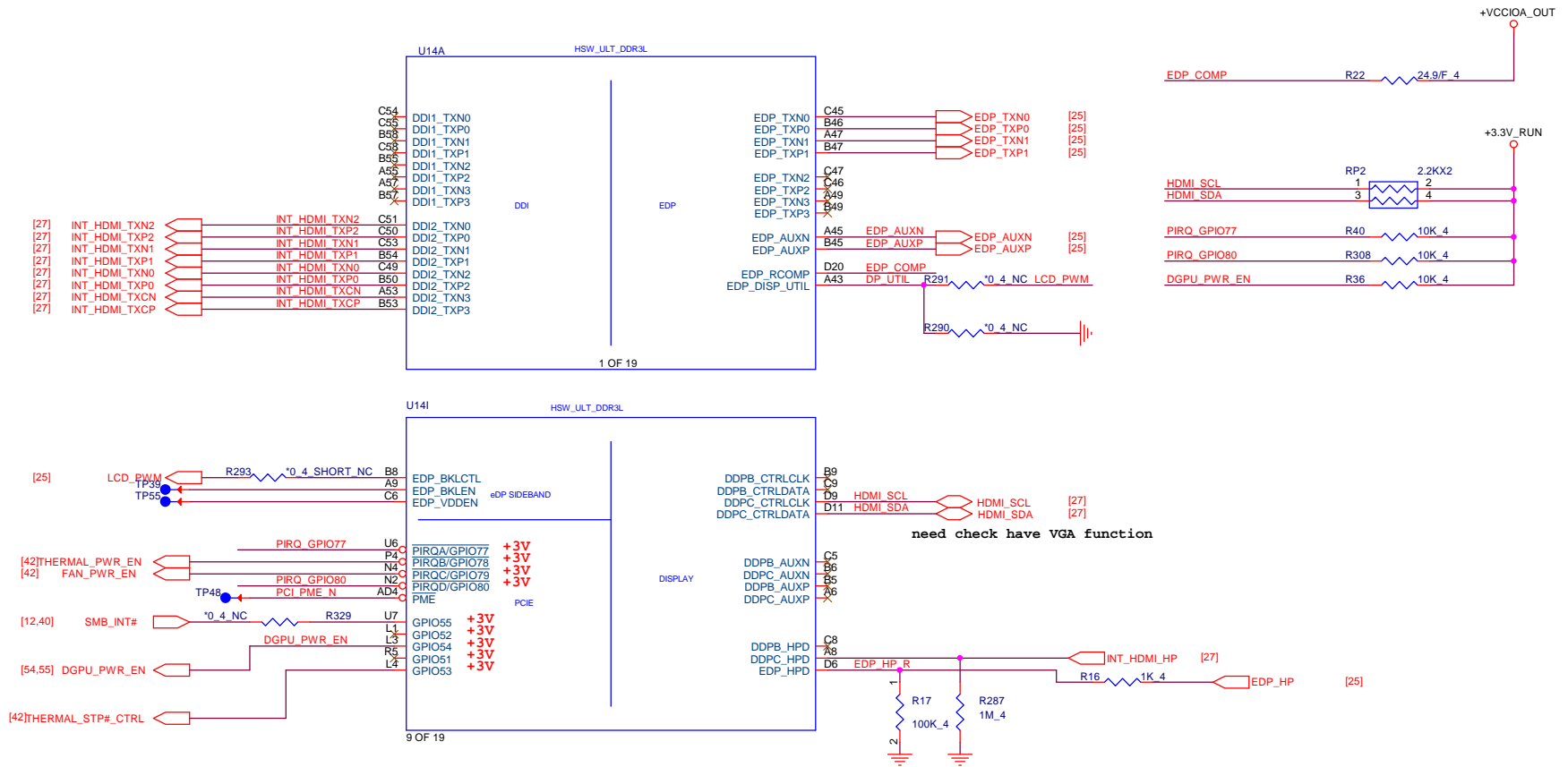
Power Sequence
(G3 to S0)

Shark Bay ULT PSS, 490828, Rev1.1



WWW.AliSaler.Com

Haswell ULT (DISPLAY)



Quanta Computer Inc.
PROJECT : JW8B

Haswell ULT (DDR3L)

U14C

HSW_ULT_DDR3L

AH63	SA_DQ0	AU37
AH62	SA_DQ1	AV37
AK63	SA_CLK0	AW36
AK62	SA_CLK#1	AY36
AH61	SA_CLK1	AX36
AH60	SA_DQ4	AU43
SA_DQ5	SA_CKE0	AW43
AK61	SA_CKE1	AY42
AK60	SA_DQ7	AY43
AM63	SA_DQ8	AY43
AM62	SA_CKE2	AY43
AP63	SA_CKE3	AY43
AP62	SA_CS#0	AP33
AM61	SA_CS#1	AR32
AM60	SA_ODT0	AP32
AP61	SA_ODT0	AP32
AP60	SA_ODT0	AP32
AP59	SA_ODT0	AP32
AP58	SA_ODT0	AP32
AR58	SA_ODT0	AP32
AM57	SA_ODT0	AP32
AK57	SA_ODT0	AP32
AL58	SA_ODT0	AP32
AK58	SA_ODT0	AP32
AR57	SA_ODT0	AP32
AN57	SA_ODT0	AP32
AP56	SA_ODT0	AP32
AR56	SA_ODT0	AP32
AM54	SA_ODT0	AP32
AK54	SA_ODT0	AP32
AL55	SA_ODT0	AP32
AK55	SA_ODT0	AP32
AR54	SA_ODT0	AP32
AN54	SA_ODT0	AP32
AY58	SA_ODT0	AP32
AY56	SA_ODT0	AP32
AW58	SA_ODT0	AP32
AW56	SA_ODT0	AP32
AV58	SA_ODT0	AP32
AU58	SA_ODT0	AP32
AV56	SA_ODT0	AP32
AU56	SA_ODT0	AP32
AY54	SA_ODT0	AP32
AW54	SA_ODT0	AP32
AY52	SA_ODT0	AP32
AW52	SA_ODT0	AP32
AV54	SA_ODT0	AP32
AU54	SA_ODT0	AP32
AV52	SA_ODT0	AP32
AU52	SA_ODT0	AP32
AK49	SA_ODT0	AP32
AK42	SA_ODT0	AP32
AM43	SA_ODT0	AP32
AM45	SA_ODT0	AP32
AK45	SA_ODT0	AP32
AK43	SA_ODT0	AP32
AM40	SA_ODT0	AP32
AM42	SA_ODT0	AP32
AM46	SA_ODT0	AP32
AK46	SA_ODT0	AP32
AM49	SA_ODT0	AP32
AK49	SA_ODT0	AP32
AM48	SA_ODT0	AP32
AK48	SA_ODT0	AP32
AM51	SA_ODT0	AP32
AK51	SA_ODT0	AP32
SA_DQ63	SA_DQ63	SA_DQ63

DDR CHANNEL A

3 OF 19

[19] M_B_DQ[63..0]

U14D


HSW_ULT_DDR3L

M_B_DQ0	AY31
M_B_DQ1	AW31
M_B_DQ2	AY29
M_B_DQ3	AW29
M_B_DQ4	AV31
M_B_DQ5	AU31
M_B_DQ6	AV29
M_B_DQ7	AU29
M_B_DQ8	AY27
M_B_DQ9	AW27
M_B_DQ10	AY25
M_B_DQ11	AW25
M_B_DQ12	AV27
M_B_DQ13	AU27
M_B_DQ14	AV25
M_B_DQ15	AU25
M_B_DQ16	AM29
M_B_DQ17	AK29
M_B_DQ18	AL28
M_B_DQ19	AK28
M_B_DQ20	AR29
M_B_DQ21	AN29
M_B_DQ22	AR28
M_B_DQ23	AP28
M_B_DQ24	AN26
M_B_DQ25	AR26
M_B_DQ26	AR25
M_B_DQ27	AP25
M_B_DQ28	AK26
M_B_DQ29	AM26
M_B_DQ30	AK25
M_B_DQ31	AL25
M_B_DQ32	AY23
M_B_DQ33	AW23
M_B_DQ34	AY21
M_B_DQ35	AW21
M_B_DQ36	AV23
M_B_DQ37	AU23
M_B_DQ38	AV21
M_B_DQ39	AU21
M_B_DQ40	AY19
M_B_DQ41	AW19
M_B_DQ42	AY17
M_B_DQ43	AW17
M_B_DQ44	AV19
M_B_DQ45	AU19
M_B_DQ46	AV17
M_B_DQ47	AU17
M_B_DQ48	AR21
M_B_DQ49	AR22
M_B_DQ50	AL21
M_B_DQ51	AM22
M_B_DQ52	AN22
M_B_DQ53	AP21
M_B_DQ54	AK21
M_B_DQ55	AK22
M_B_DQ56	AN20
M_B_DQ57	AR20
M_B_DQ58	AK18
M_B_DQ59	AL18
M_B_DQ60	AK20
M_B_DQ61	AM20
M_B_DQ62	AR18
M_B_DQ63	AP18

DDR CHANNEL B

4 OF 19

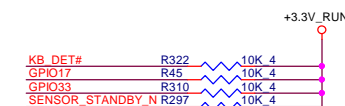
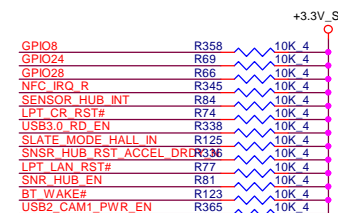
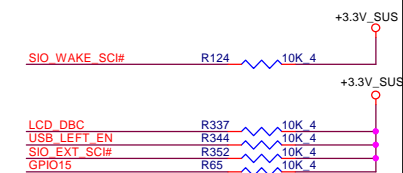
Check if not used. NC ?
12/25 Del SM_VREF_DQ0



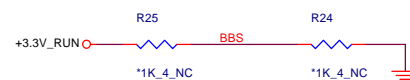
Quanta Computer Inc.
PROJECT : JW8B

Size	Document Number	Rev A
Haswell ULT 2/12		
Date:	Friday, May 10, 2013	Sheet 8 of 57

GPIO Pull-up/Pull-down(CLG)



GPIO86:Boot BIOS Strap Bit	
PU	LPC
PD	SPI (Default IPD)



GPIO66 : Top-Block Swap	
R1547	ENABLE
R1547_NC	DISABLE(Default)



Haswell ULT (PCIE,USB)

U14K

HSW_ULT_DDR3L

PCIE

USB

11 OF 19

GPU

GIGA LAN

WIFI

USB3.0 Port (Left)

Cardreader

USB3.0 Port (Power Share)

USB3.0 Port (Right)

USB3.0 Port (Left)

Finger Print

Camera

eTP Touch Panel

Bluetooth

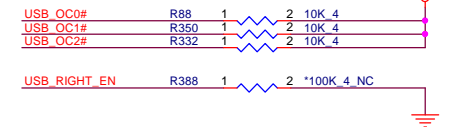
Touch Panel (JW8)

USB3.0 Port (Power Share)

USB3.0 Port (Right)

HARRIS_BEACH_CS REV 3.0

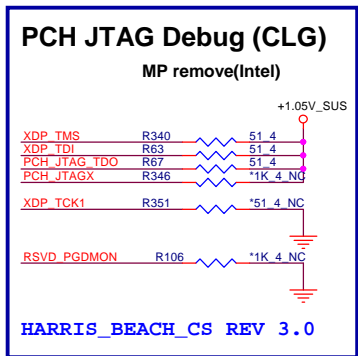
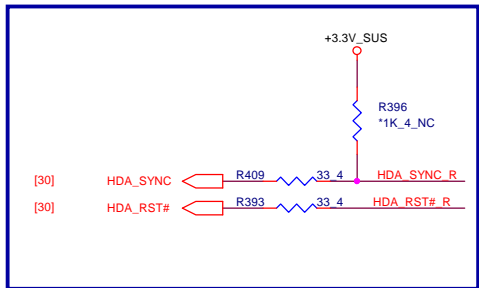
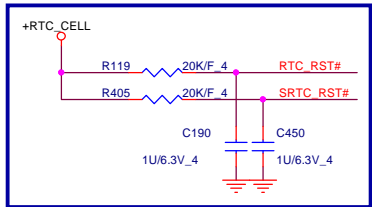
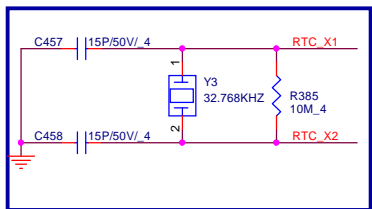
+3.3V_SUS



Quanta Computer Inc.

PROJECT : JW8B

Size	Document Number	Rev
	Haswell ULT 4/12	A
Date:	Monday, July 08, 2013	Sheet 10 of 57

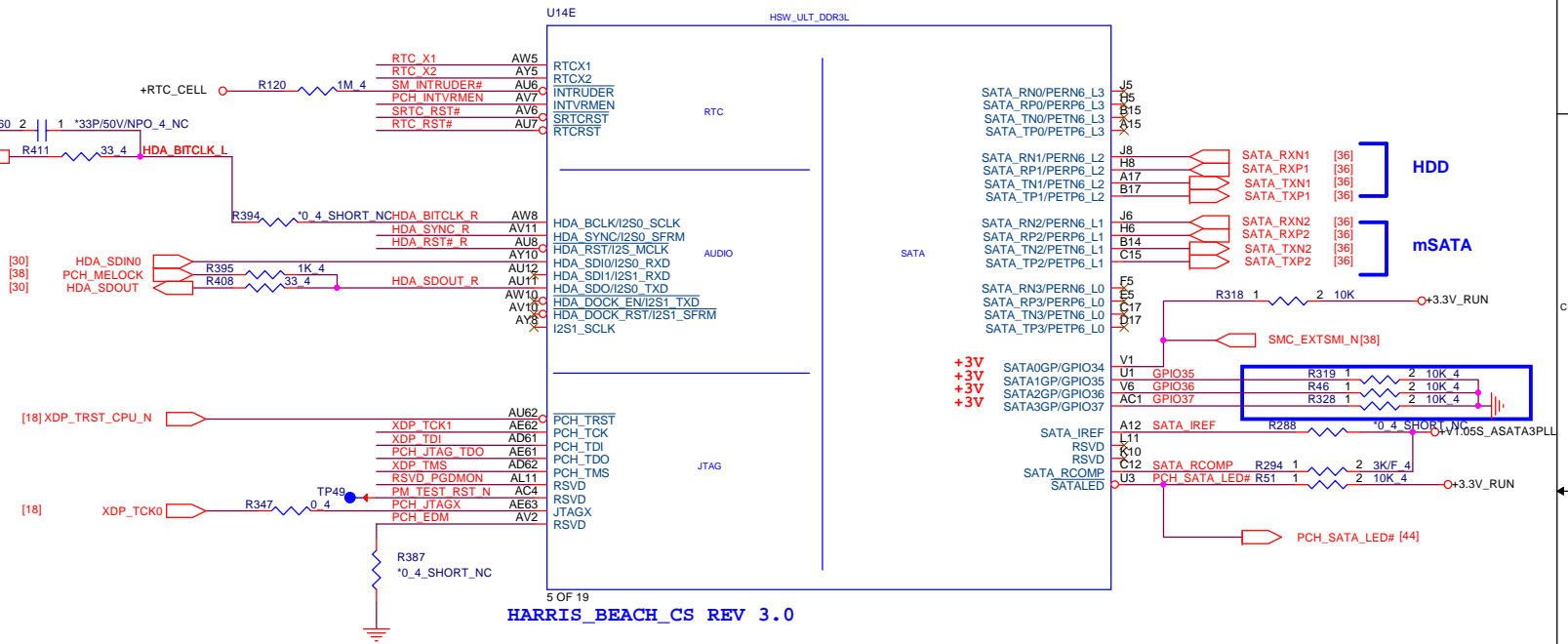


DFXTESTMODE
HIGH - DFXTESTMODE DISABLED(DEFAULT)
LOW - DFXTESTMODE ENABLED

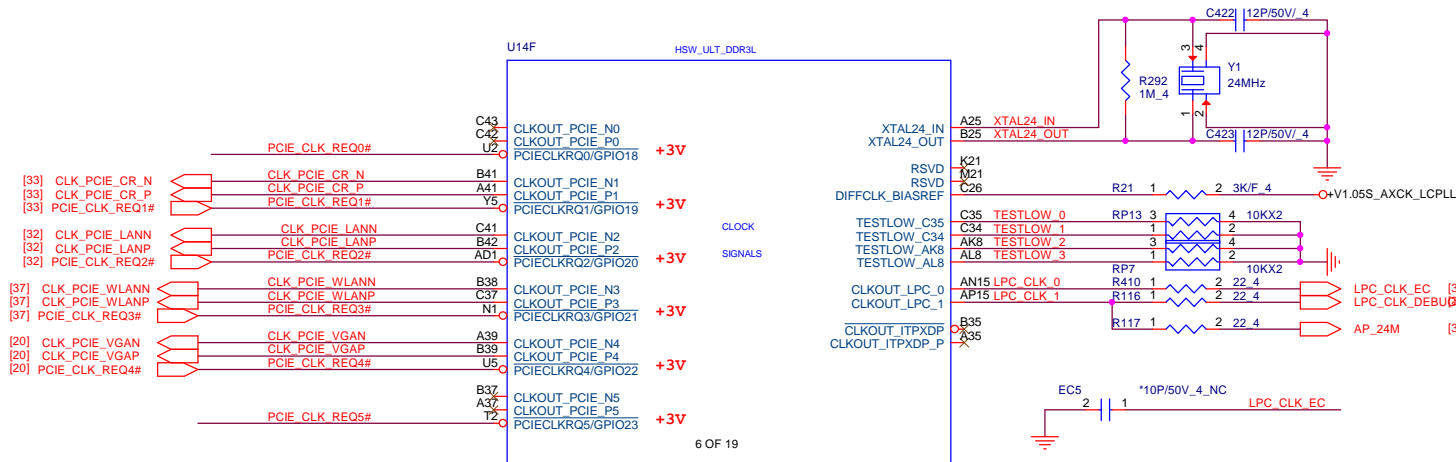
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL ○ R407 ○ *330K_4_NC PCH_INTVRMEN R392 ○ 330K_4

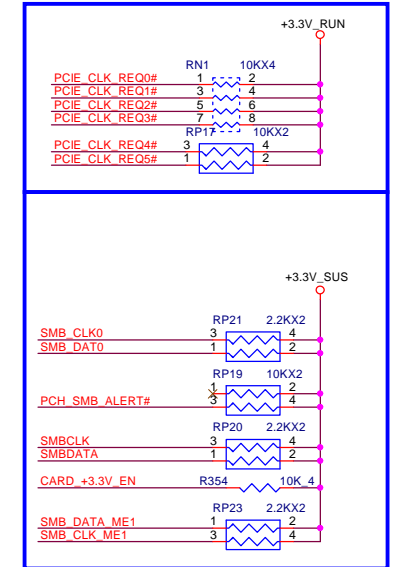
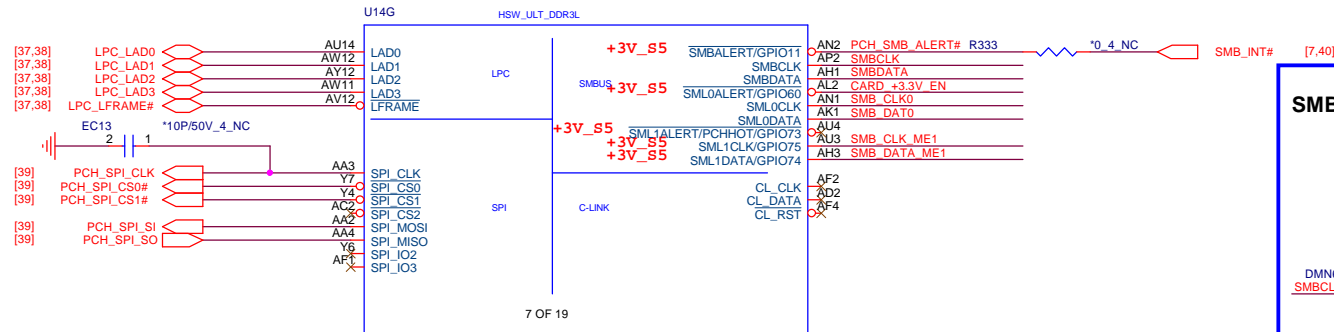
Haswell ULT (RTC, HDA, JTAG, SATA)



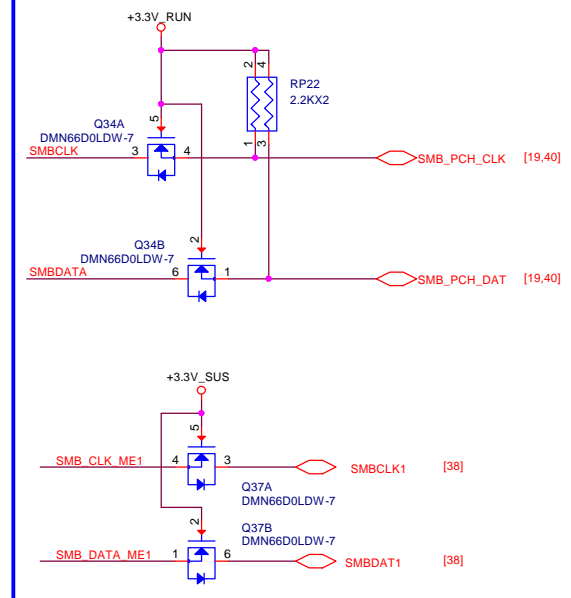
Haswell ULT (CLK)



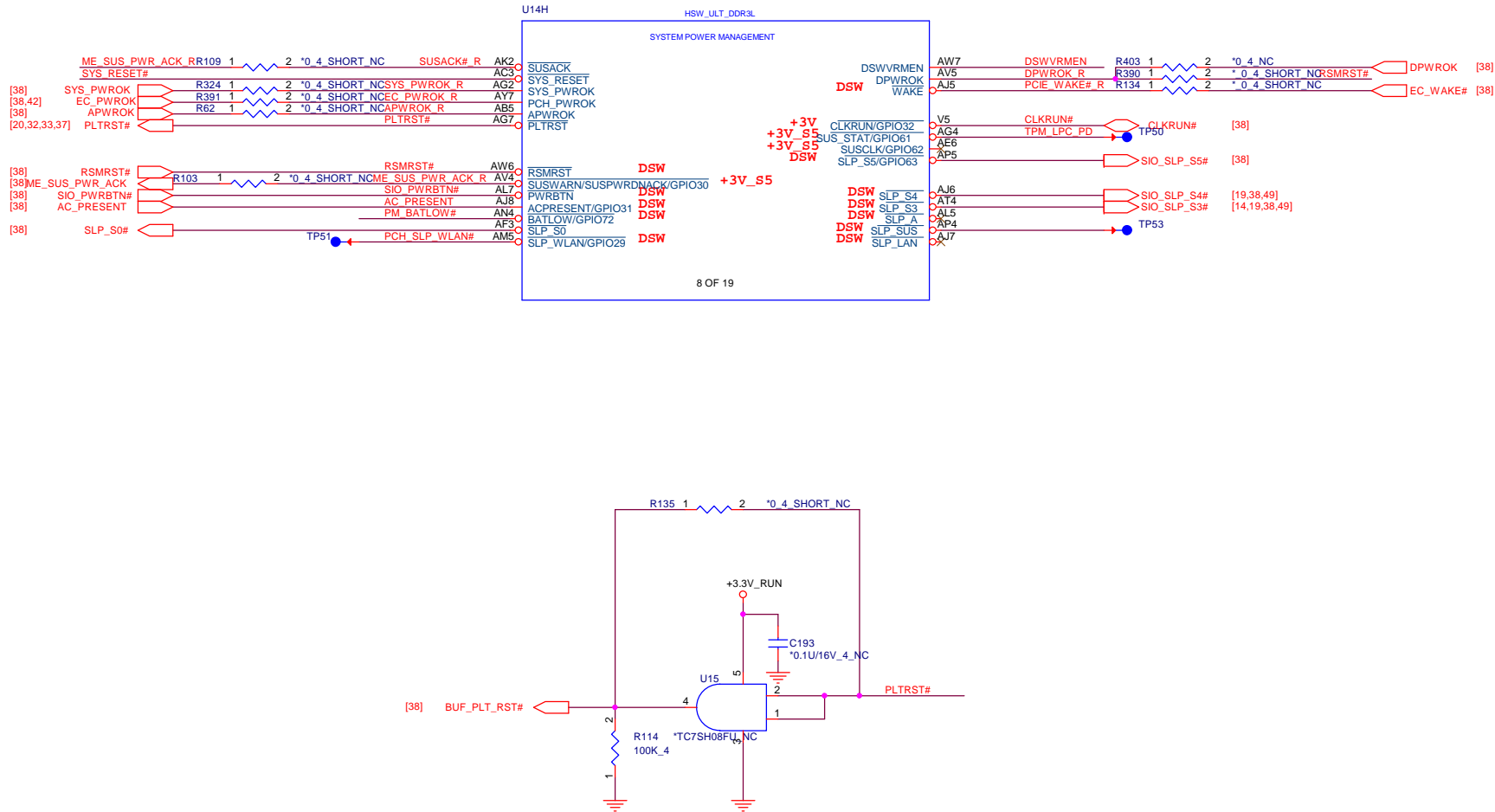
Haswell ULT (LPC/SPI/SMB/CLINK)



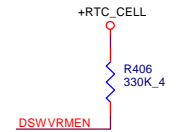
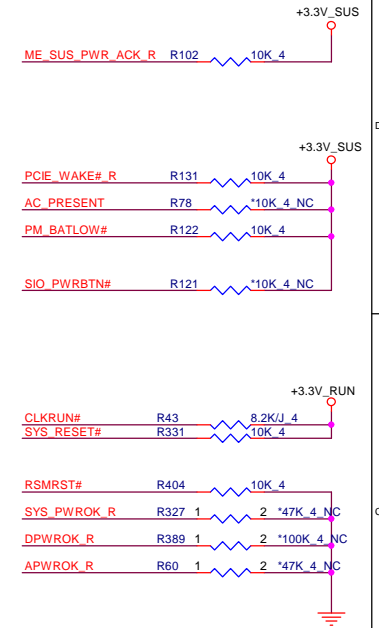
SMBus/Pull-up(CLG)



Haswell ULT (SYSTEM POWER MANAGEMENT)



PCH Pull-high/low(CLG)



On Die DSW VR Enable
High = Enable (Default)
Low = Disable



Quanta Computer Inc.
PROJECT : JW8B

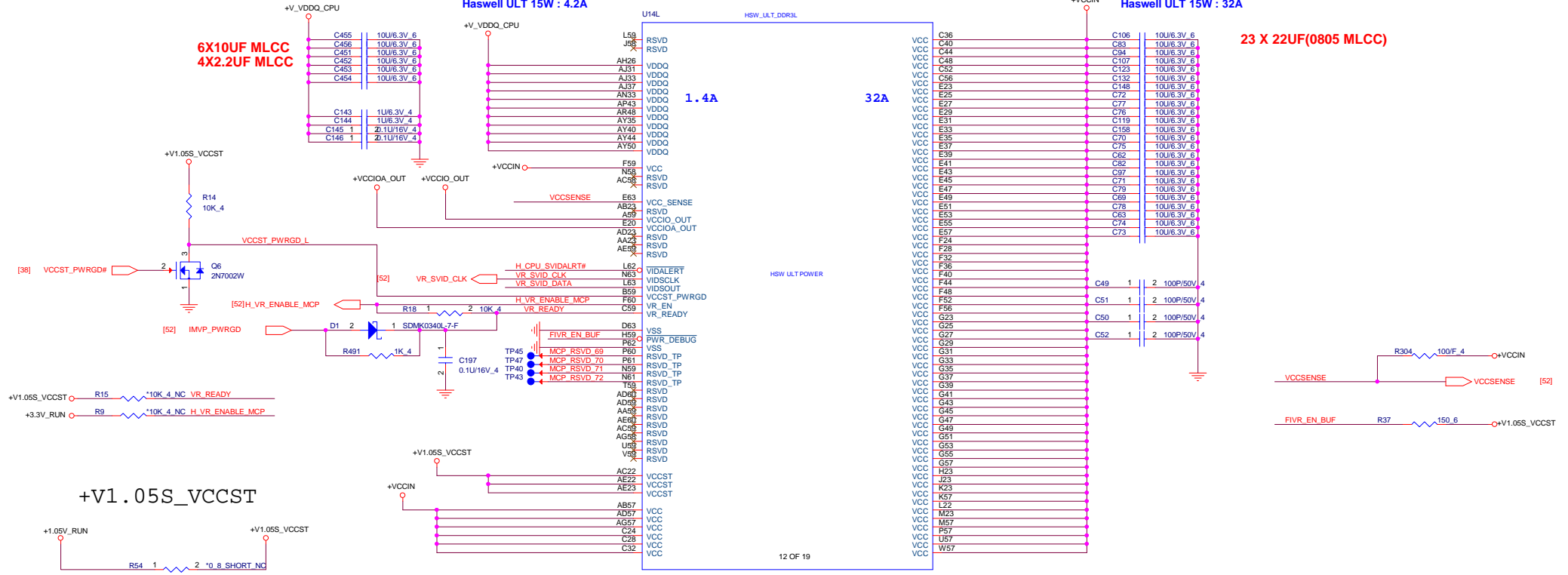
Haswell ULT MCP(POWER)

CPU VDDQ
Haswell ULT 15W : 4.2A

CPU VCC 1/21: 220uX23 --> 100uX23
Haswell ULT 15W : 32A

6X10UF MLCC
4X2.2UF MLCC

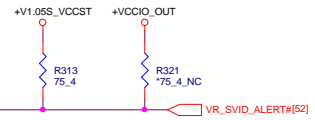
23 X 22UF(0805 MLCC)



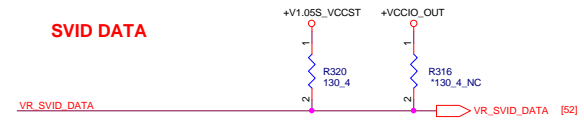
S3 Power reduce



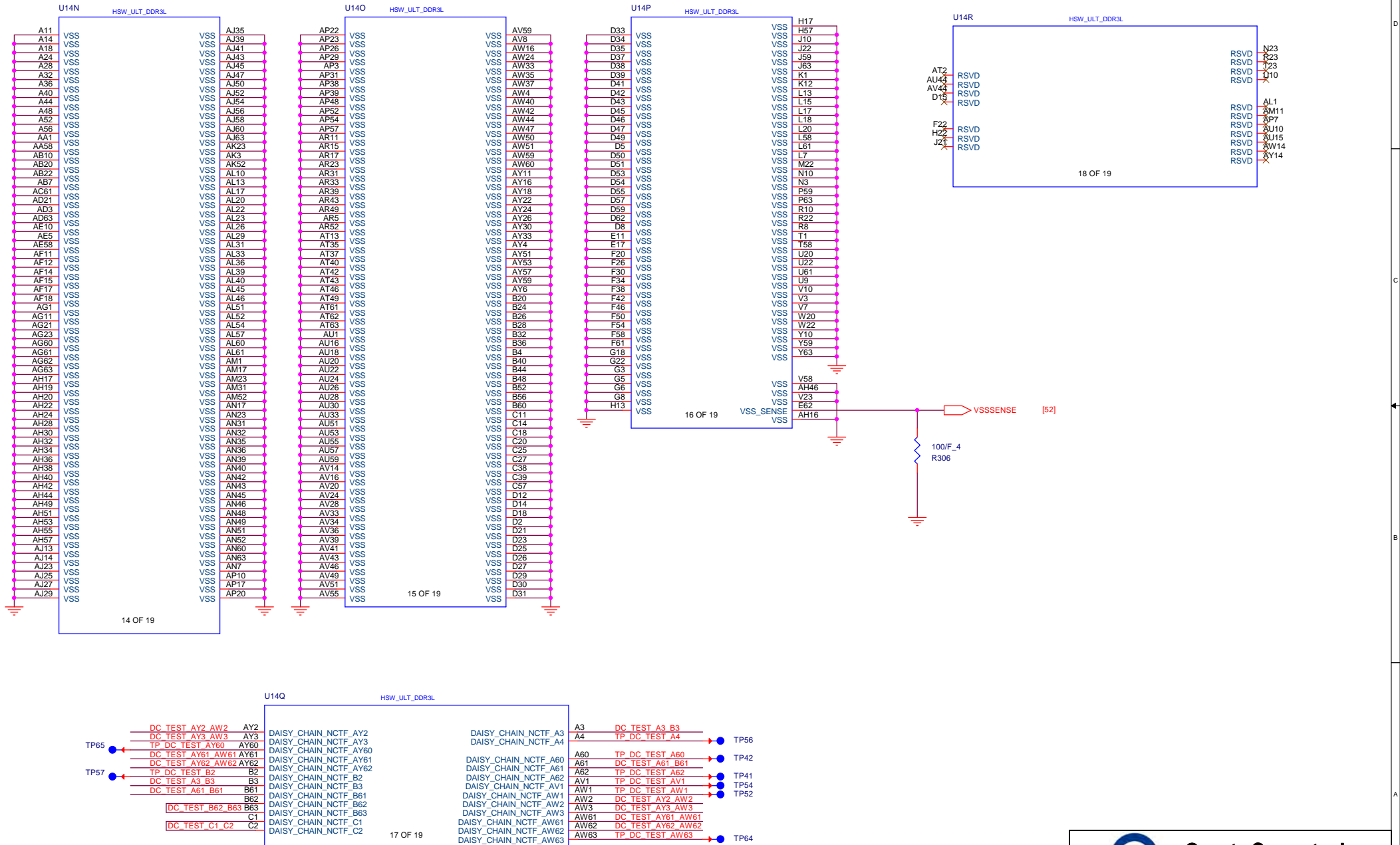
SVID ALERT



SVID DATA

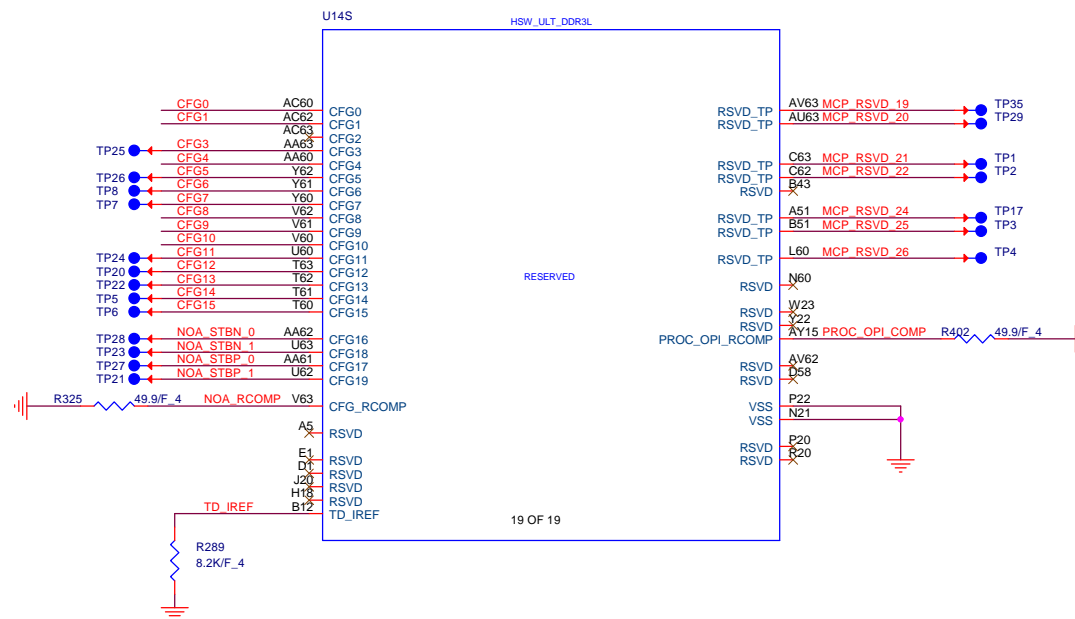


Haswell ULT (GND)

**Quanta Computer Inc.**

PROJECT : JW8B

Size	Document Number	Rev
	Haswell ULT 9/12	A
Date:	Wednesday, July 17, 2013	Sheet 15 of 57



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R339 *1K 4 NC
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R334 *1K 4 NC
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R330 *1K 4 NC
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG4 R61 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R326 *1K 4 NC
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R58 *1K 4 NC
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R57 *1K 4 NC



Quanta Computer Inc.

PROJECT : JW8B

Size	Document Number	Rev
	Haswell ULT 10/12	A
Date:	Friday, May 10, 2013	Sheet 16 of 57


```

3.3 SUS: 205mA
1.05 SUS: 2066mA
1.05 RUN: 2578mA
3.3 RUN: 58mA

```

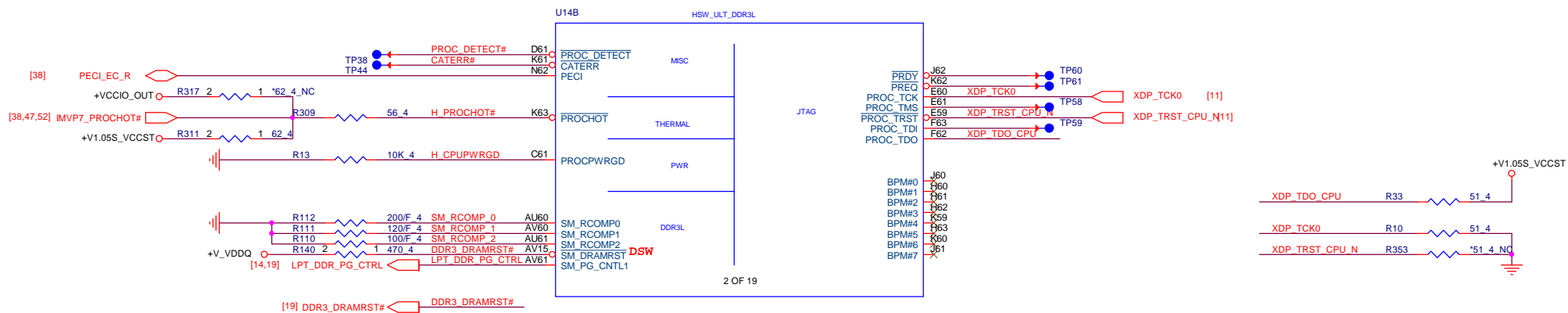


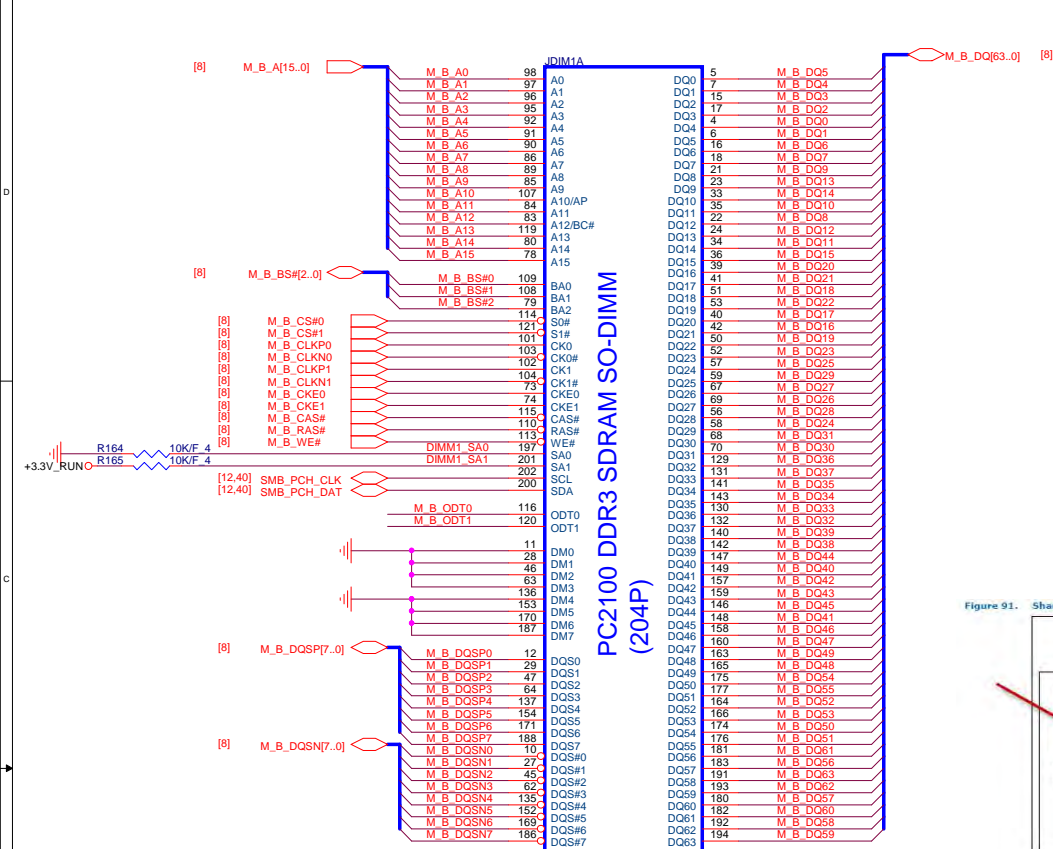
VCCSUS3
129mA

VCC1_05
2.6A

VCCASW
473mA

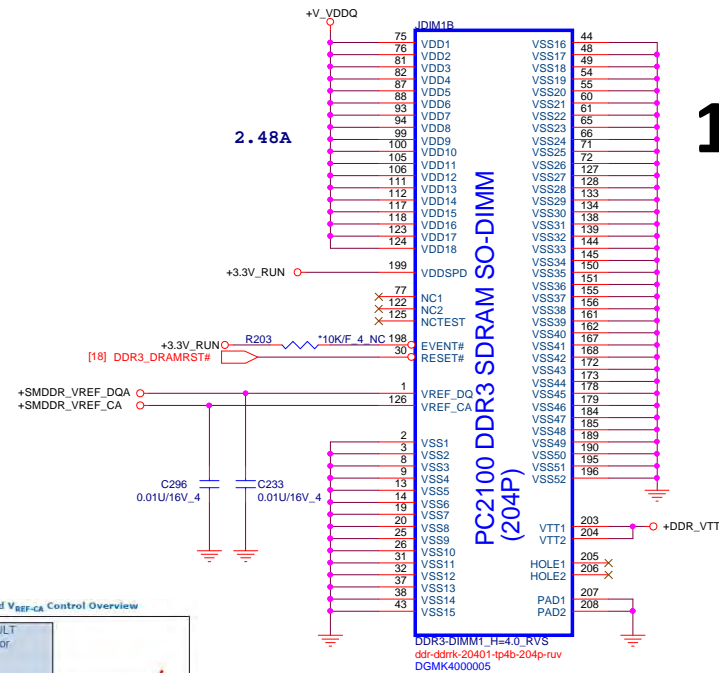
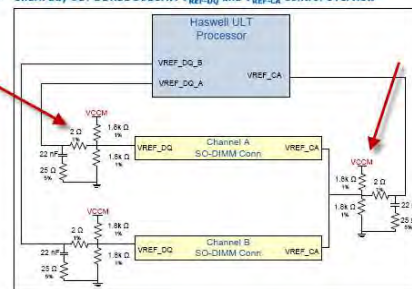




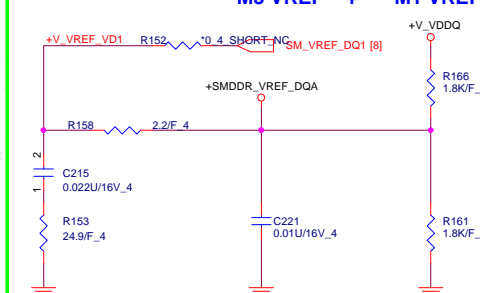


DDR3-DIMM1_H=4.0_RVS
ddr-ddrmk-20401-tp4b-204p-ruv
DGMK4000005

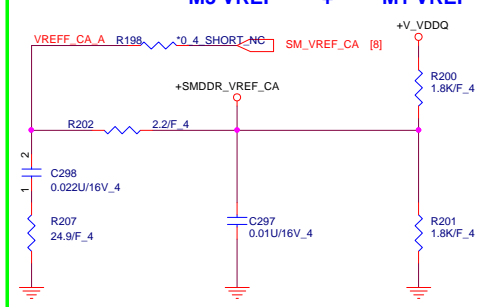
Figure 91. Shark Bay ULT DDR3L SODIMM V_{REF-DQ} and V_{REF-CA} Control Overview



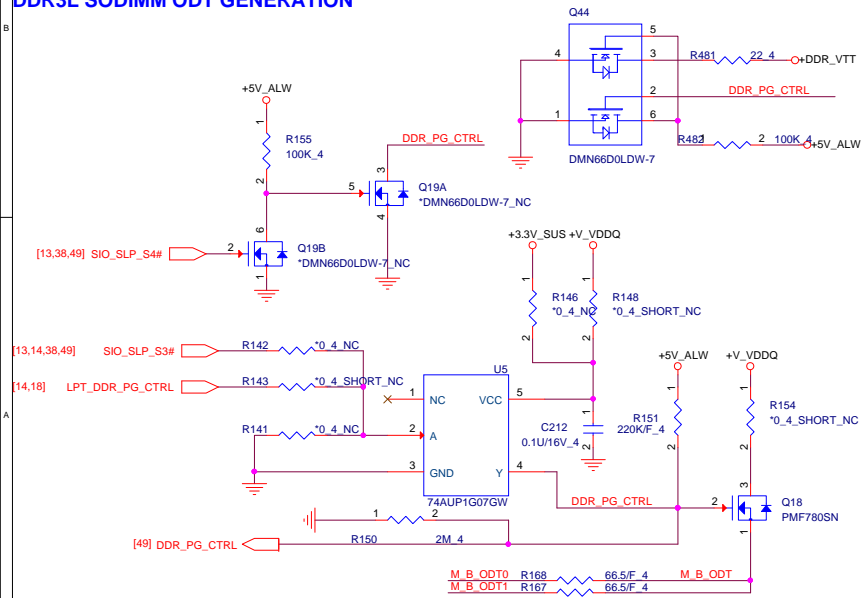
M3 VREF + M1 VREF



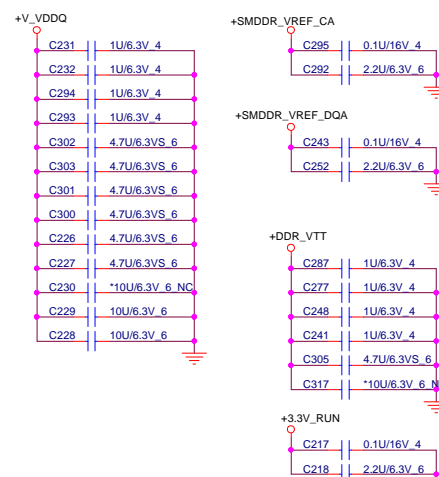
M3 VREF + M1 VREF

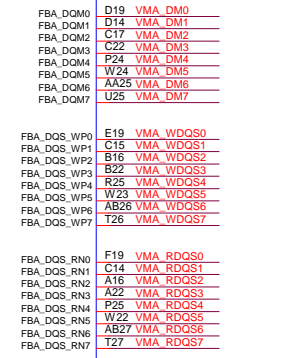
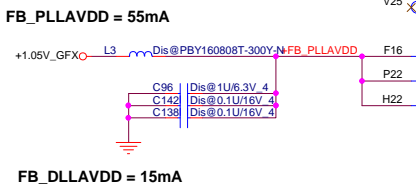
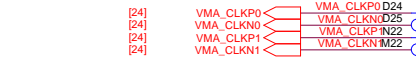
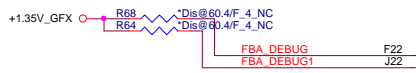
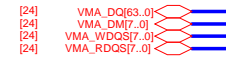
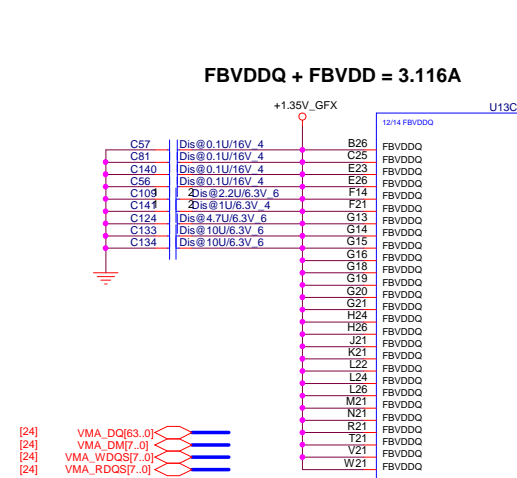
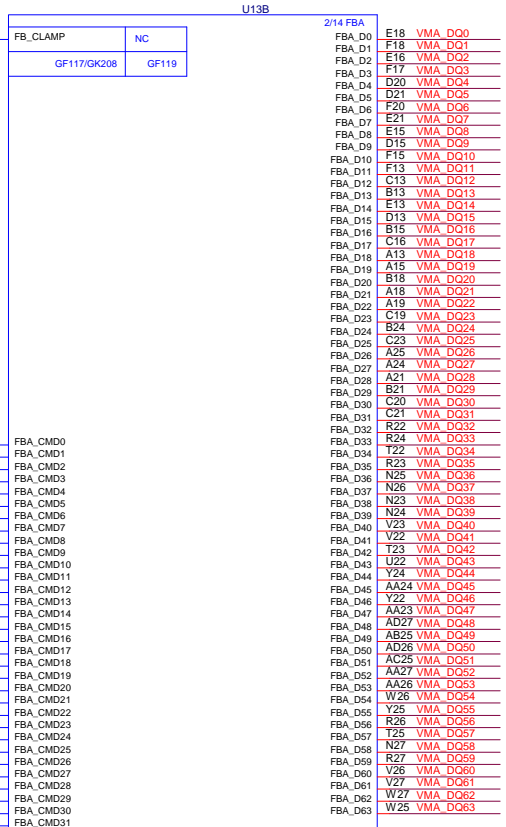
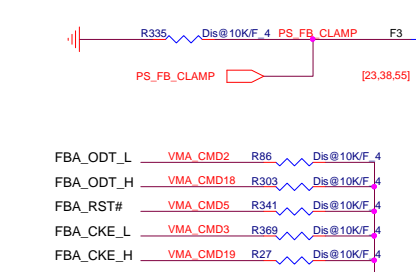


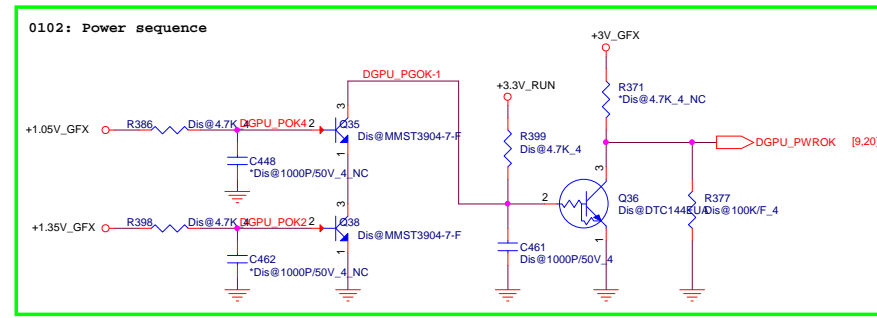
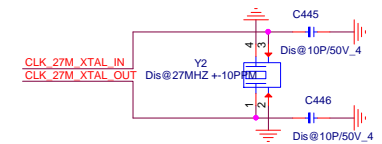
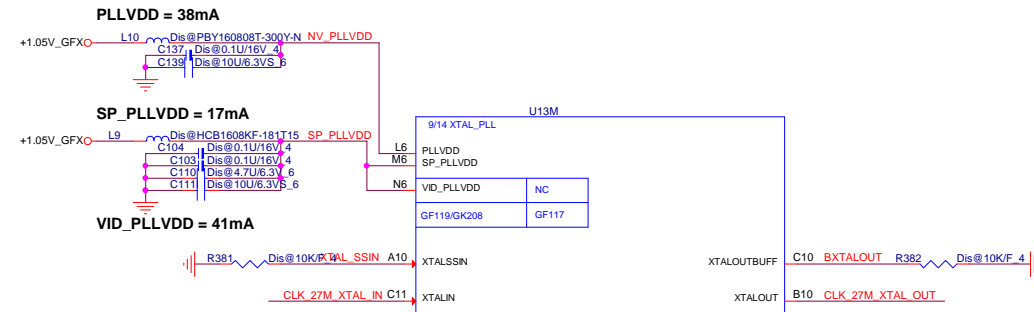
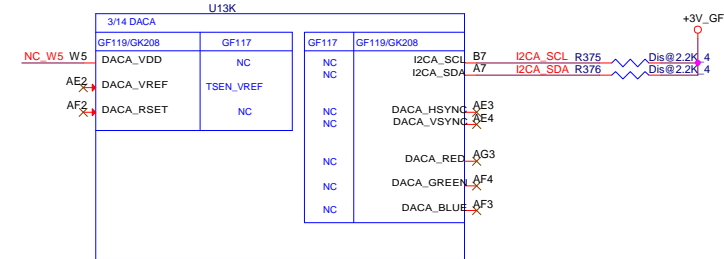
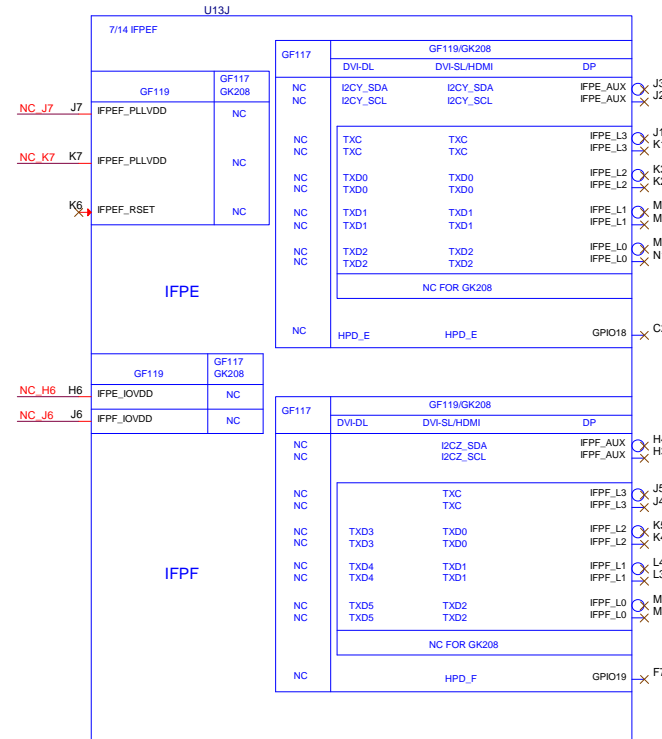
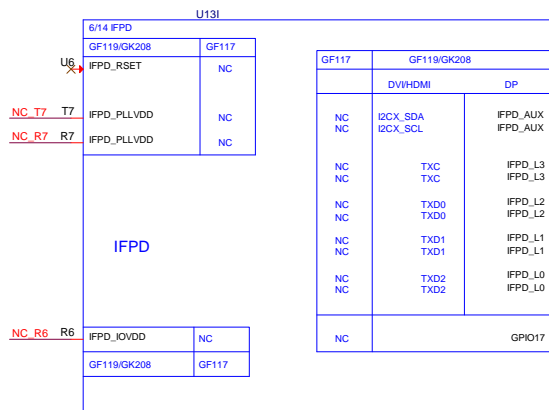
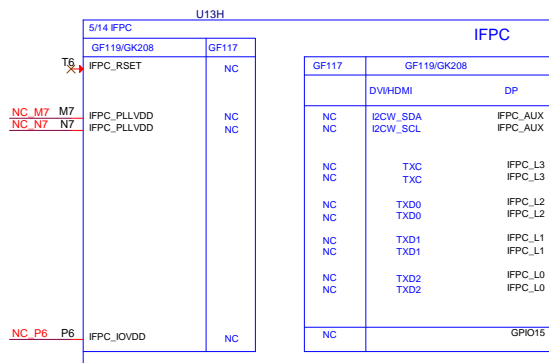
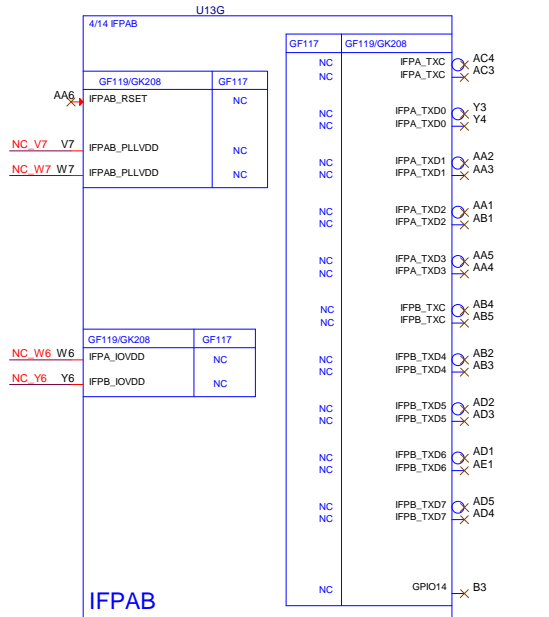
DDR3L SODIMM ODT GENERATION

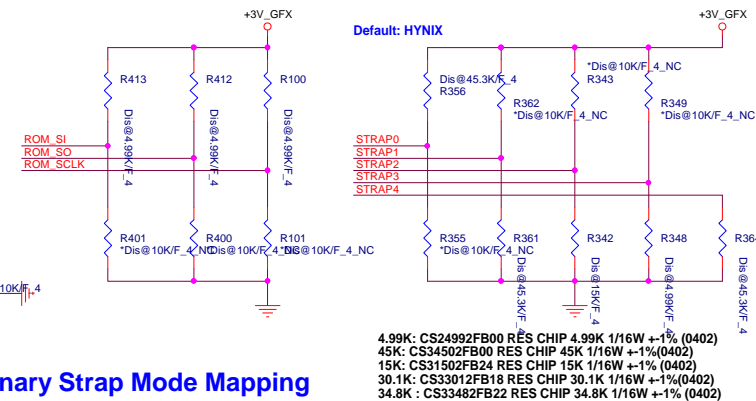
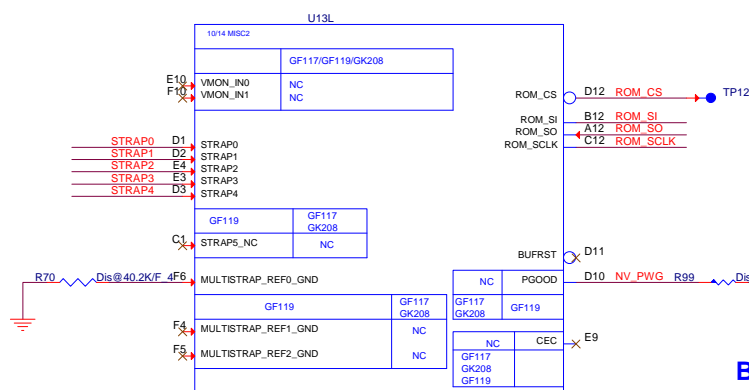


Place these Caps near So-Dimm1.









4.99K: CS24992FB00 RES CHIP 4.99K 1/16W +1% (0402)
 45K: CS34502FB00 RES CHIP 45K 1/16W +1% (0402)
 15K: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
 30.1K: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)
 34.8K: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)

Binary Strap Mode Mapping

Strap Pin name	Strap Mapping	Resistance	Note
ROM_SCLK	PCI_DEVID[4] SUB_VENOR PCI_DEVID[5] PEX_PLL_EN	5Kohm , H	1000 , SUB: no Video BIOS
ROM_SI	RAM_CFG[2] RAM_CFG[1] RAM_CFG[0]	5Kohm , H	4.99K 1000 --> Micron MT41K128M16JT-107G:K (Default) 30.1K 1101 --> Micron MT41K256M16HA-107G:E 34.8K 1110 --> Hynix H5TC4G63AFR-11C
ROM_SO	FB[1] FB[0] SMB_ALT_ADDR VGA_DEVICE	5Kohm , H	1000 , FB: 256 MB (Default) SMB:0x9E
STRAP0	User strap [3:0]	45Kohm , H	1111 , EDID is used
STRAP1	3GIO_CFG[3:0]	45Kohm , D	1111 , USER defined
STRAP2	PCI_DEVID[3:0]	15Kohm , D	010010 , N14P-GV2
STRAP3	SOR[3:0]_EXPOSED	5Kohm , D	0000 , IFPx port not use
STRAP4	RESERVED PCIE_SPEED_GEN3 PCIE_MAX_SPEED DP_PLL_VDD33V	45Kohm , D	0111 , PCIE GEN3 setting

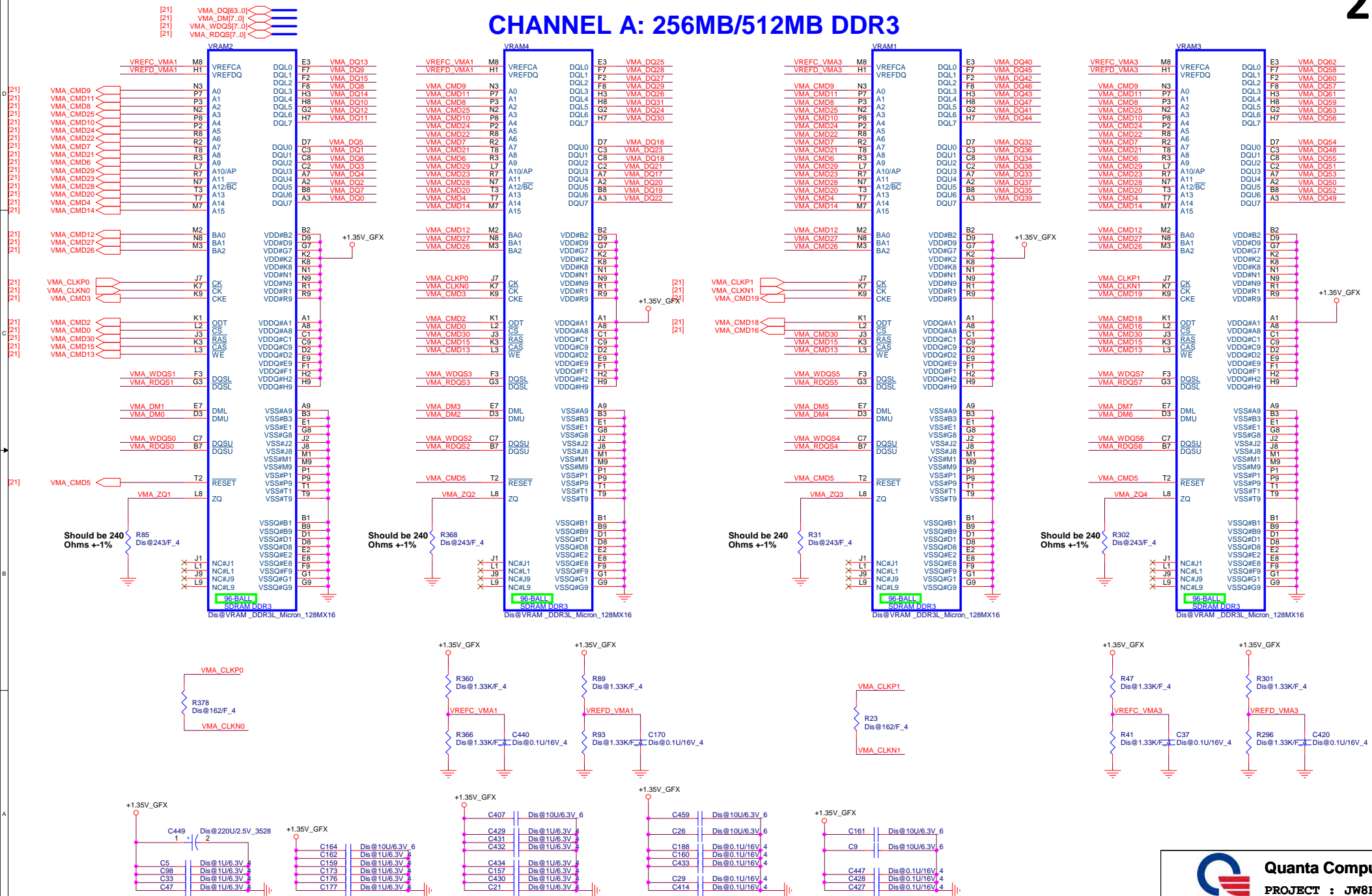
GPIO ASSIGNMENTS (GB2-64)

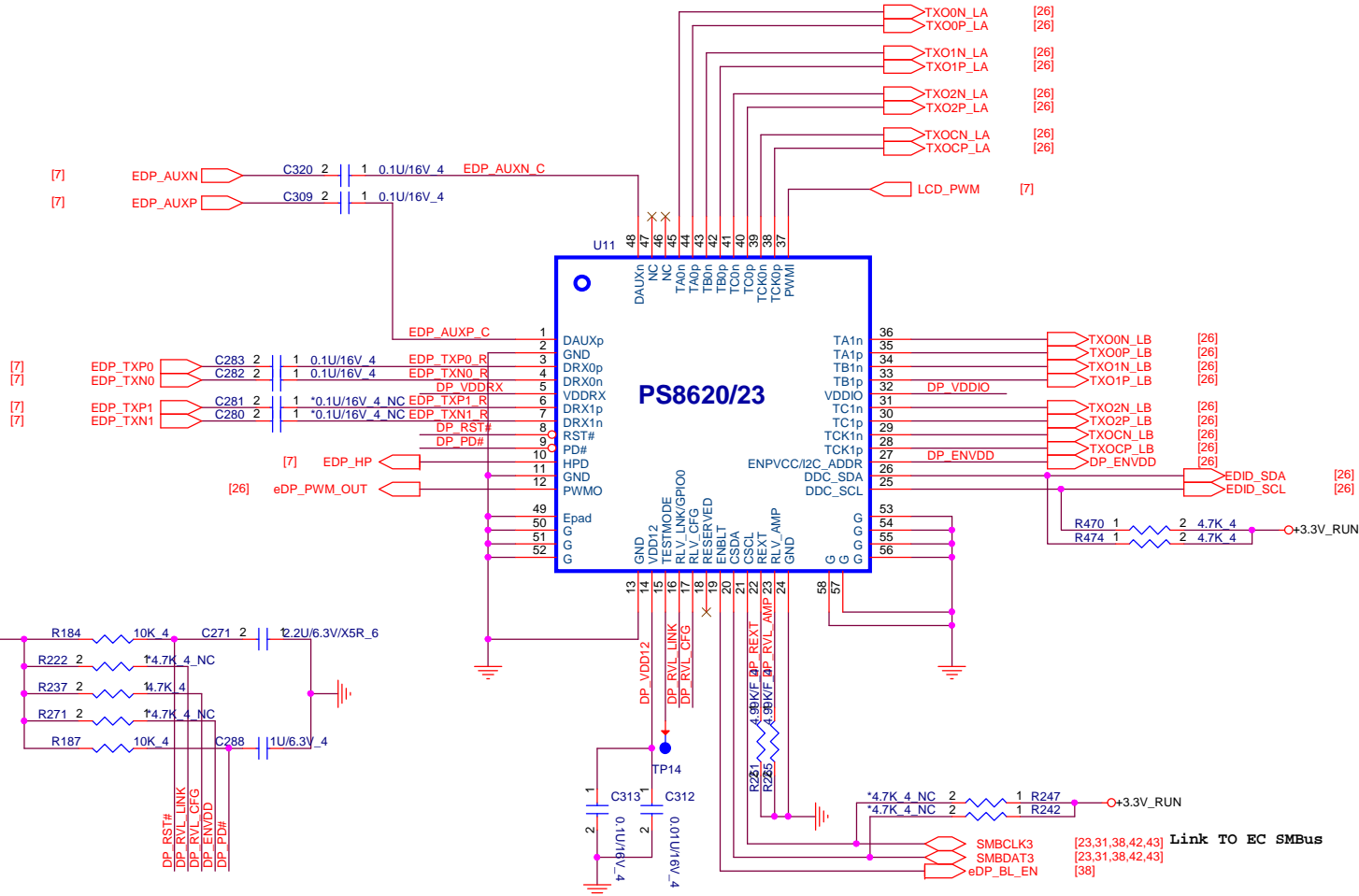
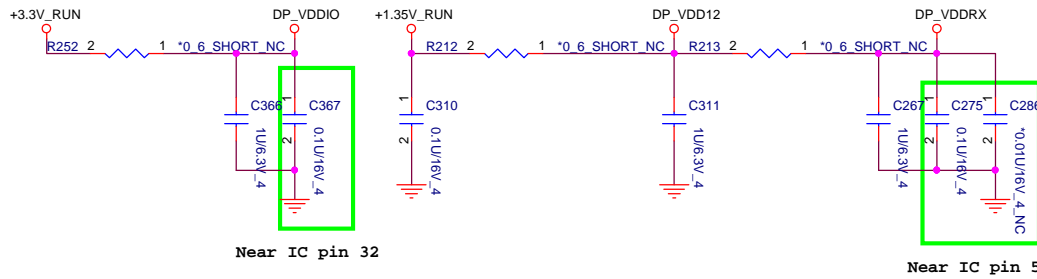
GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	MEMORY VDD ID
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5		RESERVE	
6	OUT	FB_CLAMP_TGL_REQ#	# --> FB Clamp toggle request
7	OUT	3DVision	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY VREF CONTROL
11	OUT	PWM_VID	GPU Core VDD PWM control
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	PSI	Phase Shedding
14	IN	HPD_A	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	FRM_LCK	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F or HPD_B	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	DELL P/N	QC1 P/N
0000				
1000 0x8	MT41K128M16JT-107G:K (FCBGA)(96P)	Micron	NA	AKD5DGSTL00
1101 0xD	MT41K256M16HA-107G:E	Micron	NA	AKD5PGSTL00
1110 0xE	H5TC4G63AFR-11C	Hynix	NA	AKD5PGWTW05

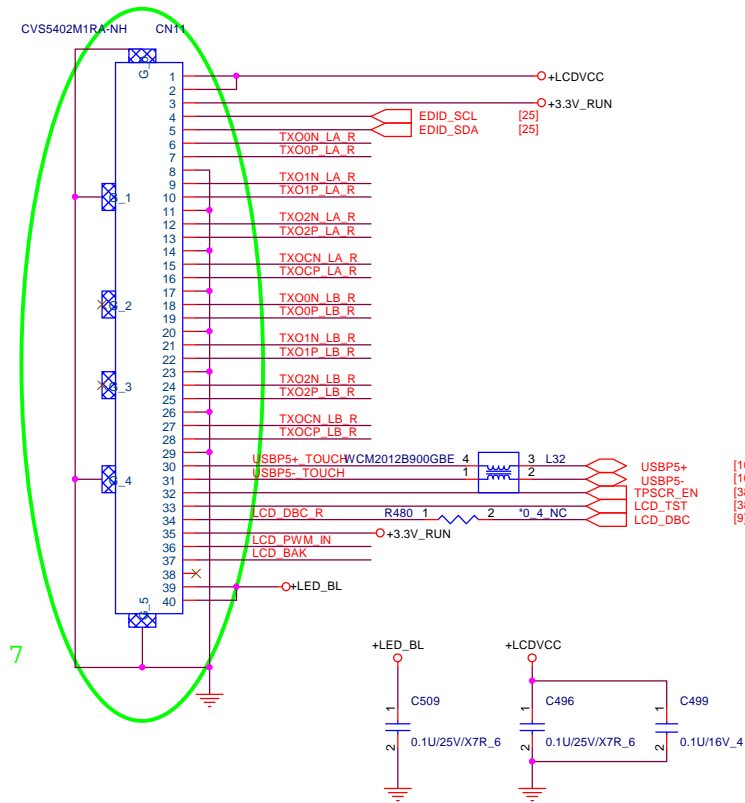
CHANNEL A: 256MB/512MB DDR3





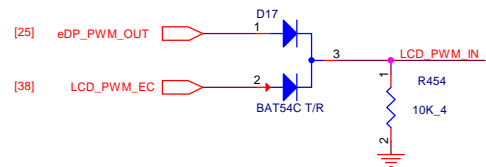
DP_ENVDD: I2C Slave address selection, internal pull-down ~80K
 L: 0x10h~0x1Fh
 H: 0x90h~0x9Fh

DP_RVL_LINK: LVDS single link or dual link selection, internal pull-down ~80K
 L: Single link LVDS
 H: Dual link LVDS

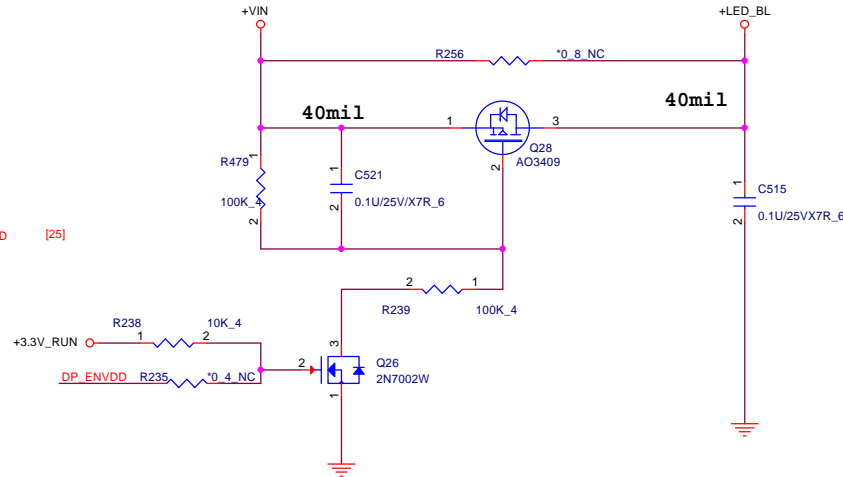
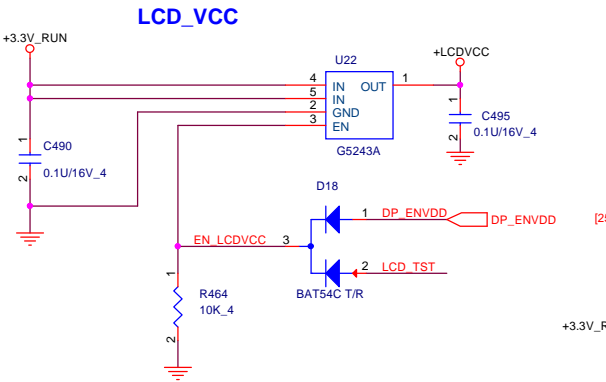
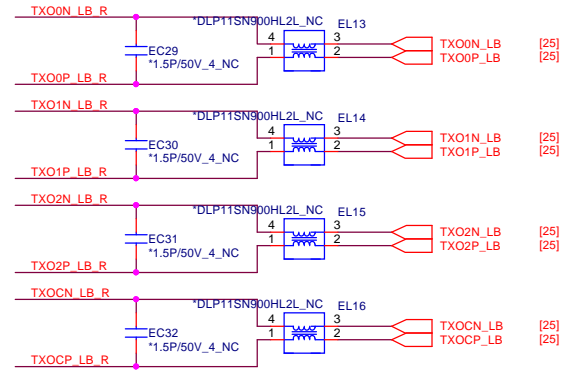
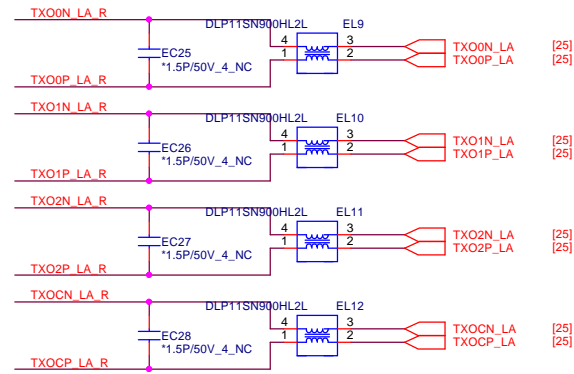
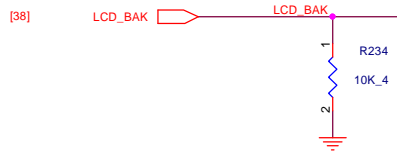


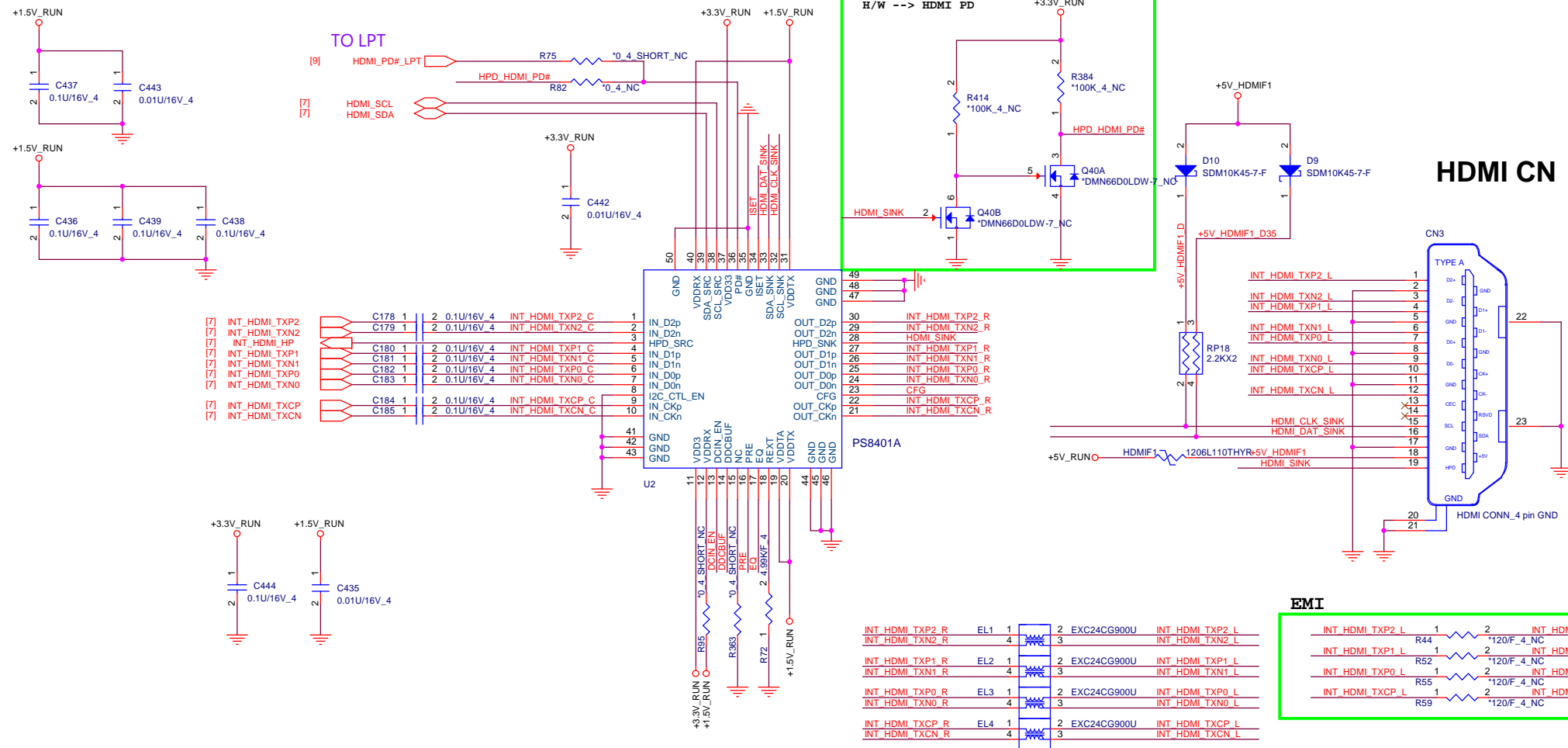
TOUCH SCREEN

Brightness Control

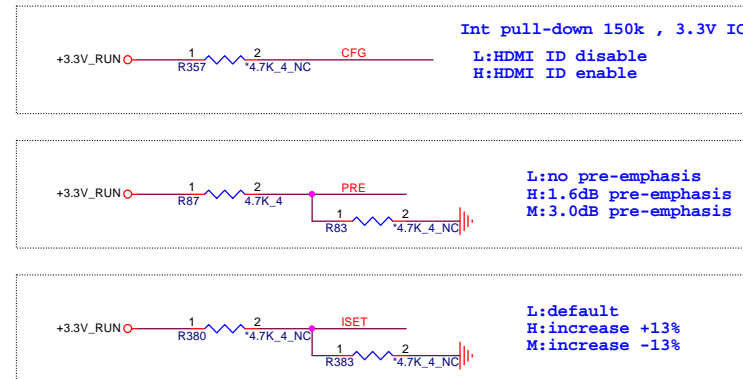
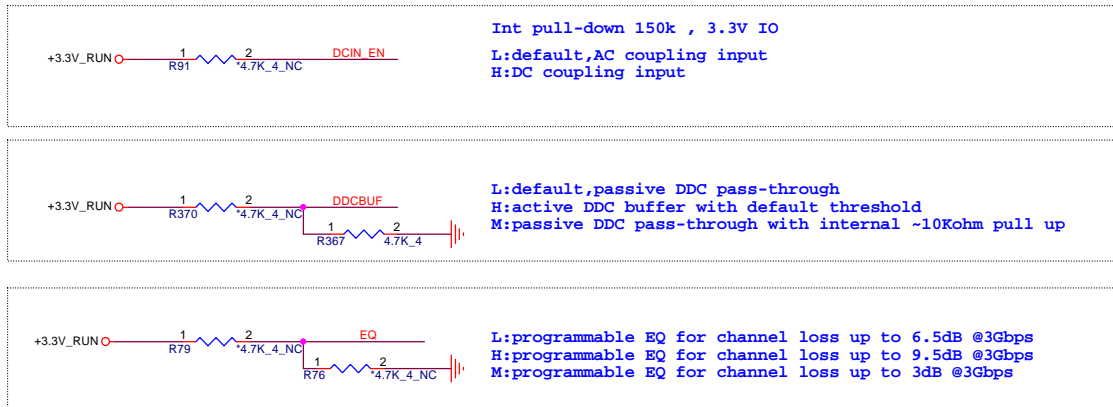


BAK_EN





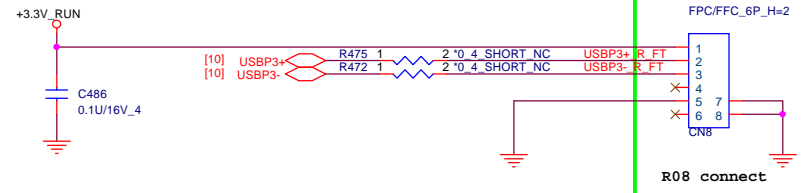
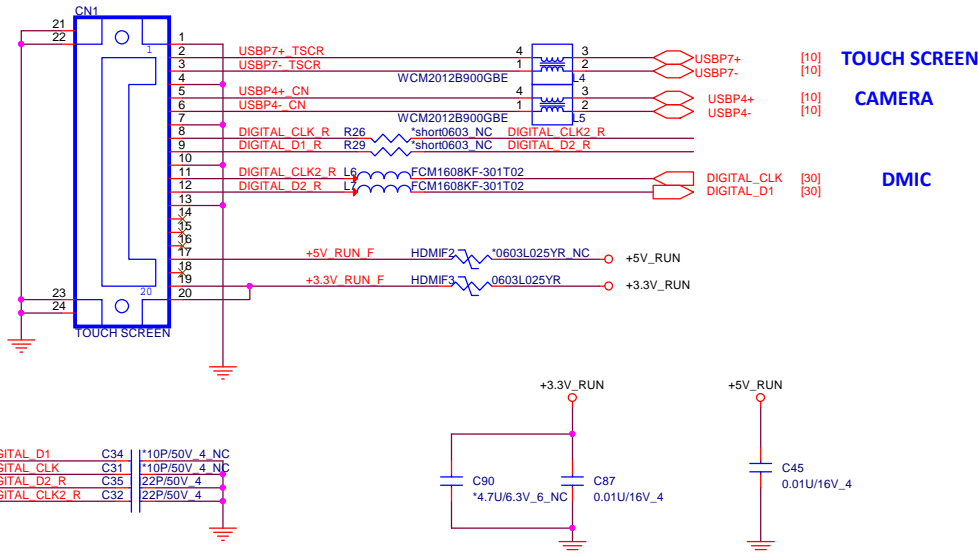
3 Level Input:
 L:LOW,internal pull down
 H:HIGH, external pull up
 M:VDD3/2, both external pill-up and pull-down



CAMERA / DMIC

Fingerprint

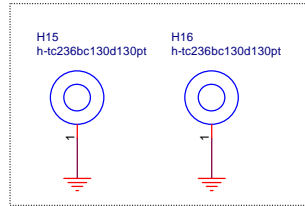
Conn P/N, Footprint OK. Luke 12/18



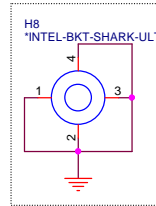
Quanta Computer Inc.
PROJECT : JW8B

Size	Document Number	Rev
	Camera/Fingerprint Conn	A
Date:	Monday, July 08, 2013	Sheet 28 of 57

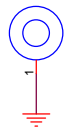
Mini-PCIE



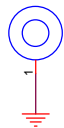
CPU BKT



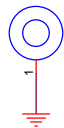
H3
*h-tc236bc315d98p2



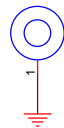
H4
*h-tc236bc315d98p2



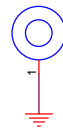
H6
*H-TSBC315D98P2



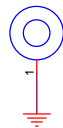
H12
*h-tc236bc315d98p2



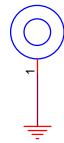
H5
*h-tc315bc150d150pt



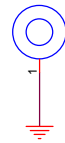
H9
*h-tc315i190bc150d150pt



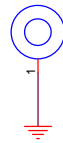
H7
*H-TC394BC315D130P2



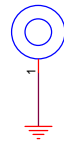
H10
*h-tc394bc315d138p2



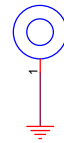
H11
*h-tc394bc315d138p2



H13
*h-tc394bc315d138p2



H14
*h-tc276bc315d118p2



H1
*h-c59d59n

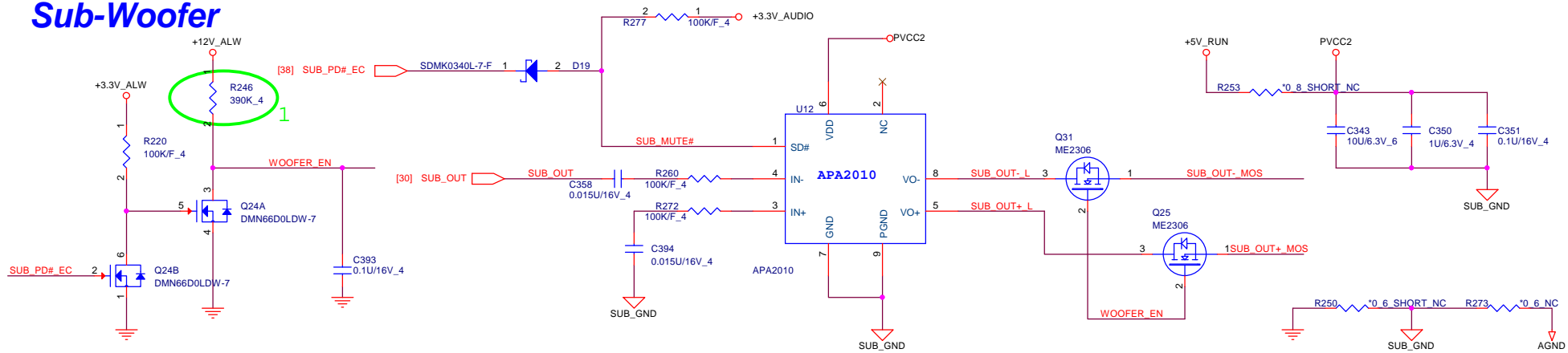


H2
*h-c59d59n

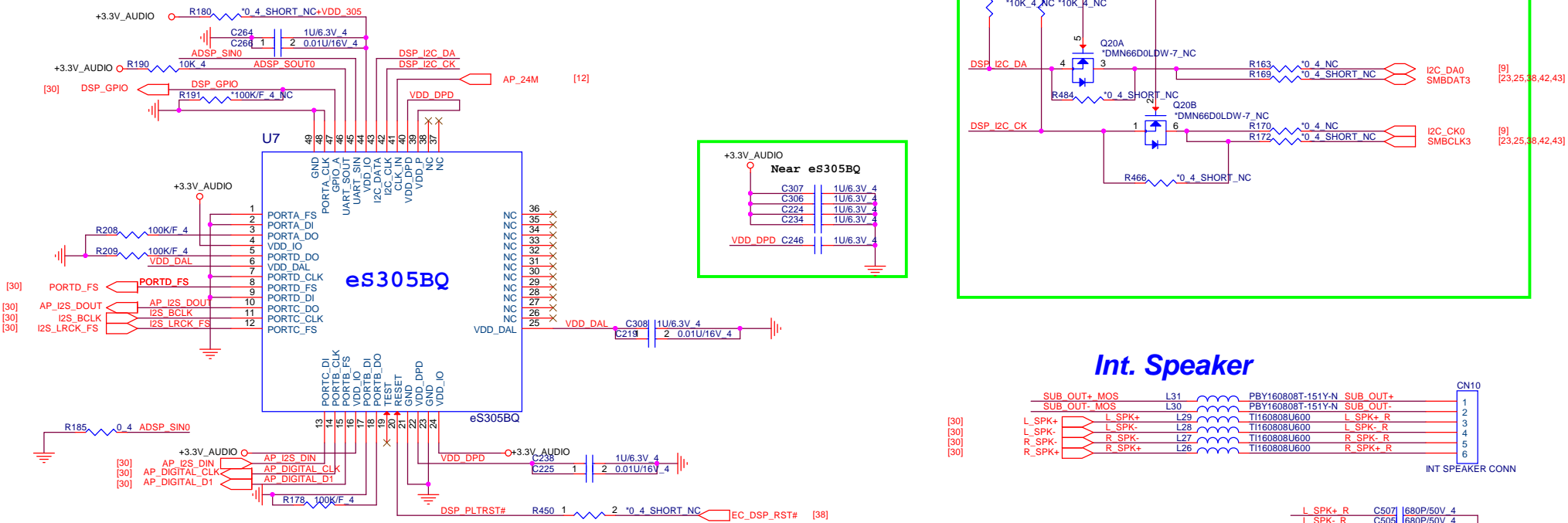


Title			
<Title>			
Size	Document Number		Rev
Custom	<Doc>		A
Date:	Friday, May 10, 2013	Sheet	29 of 57

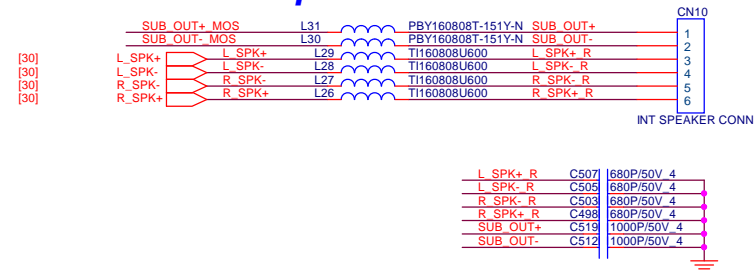
Sub-Woofer



Audio Processor



Int. Speaker



VDD10

C483 0.1U/16V 4

C480 0.1U/16V 4

C479 0.1U/16V 4

C482 0.1U/16V 4

MDIO+
MDIO-
VDD10
MDI1+
MDI1-
MDI2+
MDI2-
VDD10

U6
RTL8111G(S)/ RTL8111GUS

32 +3VLANVCC
31 RSET
30 VDD10
29 LAN_XTALO
28 LAN_XTALI
27 LAN_LED0
26 LAN_LED1
25 LAN_LED2

C249 *4.7U/6.3V_6 NC
C237 0.1U/16V 4
R441 2.49K/F

TP37
TP36
TP13

MDIP3(NC)
MDIN3(NC)
CLKREQB
HSIP
HSN
REFCLK_P
REFCLK_N
HSOP
HSON
PERSTB
SQUATEB
LANRST#
LANISOLAT#
PCIE LAN WAKE#
REG_OUT
REGOUT(NC)
LED1/IGPO
LED2(LED1)

MDIO3(NC)
MDIN3(NC)
MDI1(NC)
MDI2(NC)
AVDD10
VDD10
VDDREG(VDD33)
REGOUT(NC)

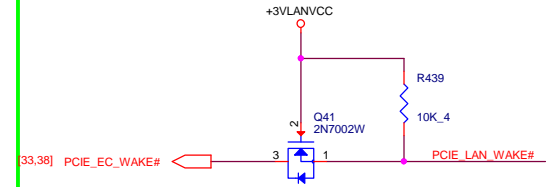
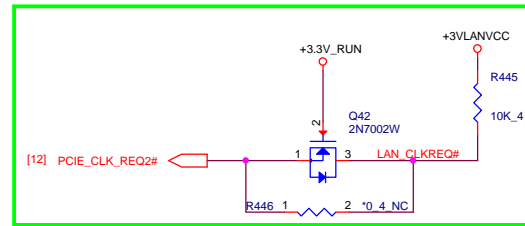
LAN RST#
LAN ISOLAT#
PCIE LAN WAKE#

VDD10
+3VLANVCC

C223 C222
C236 C251

near IC pin 22

near IC pin 23



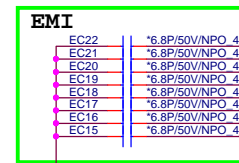
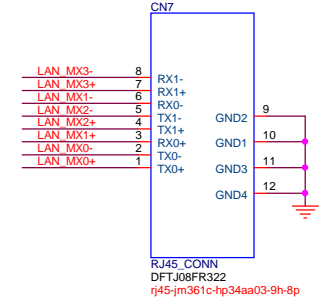
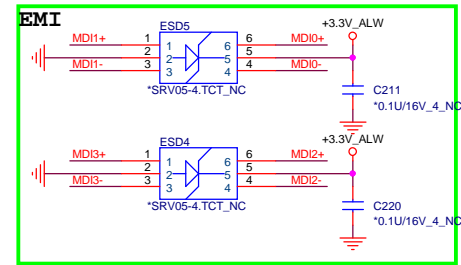
REG_OUT

L22 4.7uH_680mA_DCR=0.12 @ 7.96MHz

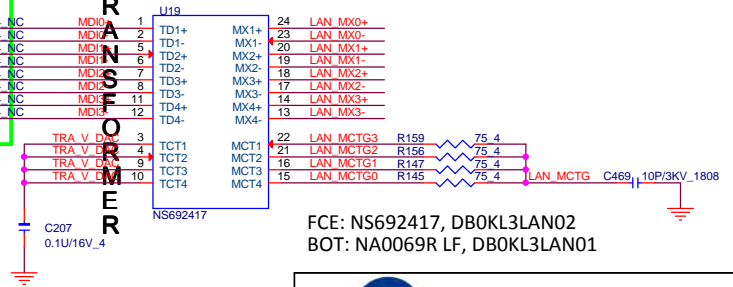
VDD10


C48 0.1uF_16V_4

C478 4.7uF_63V_6



MD10+
MD10-
MD11+
MD11-
MD12+
MD12-
MD13+
MD13-
V_DAG
V_DAG
V_DAG
V_DAG



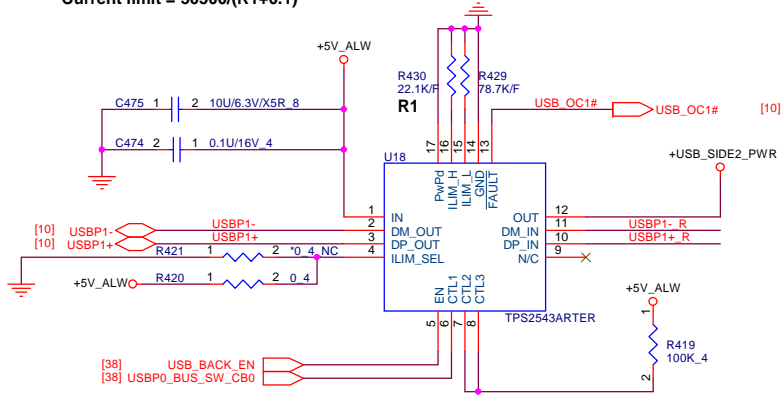
 Quanta Computer Inc. PROJECT : JW8B	
Size	Document Number LAN(RTL8111GUS)RJ45
Date: Monday, July 08, 2013	Sheet 32 of 57

USB3.0 Power Share

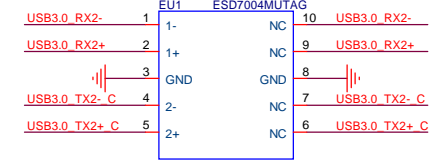
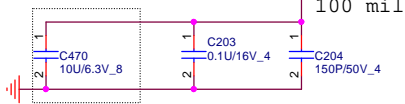
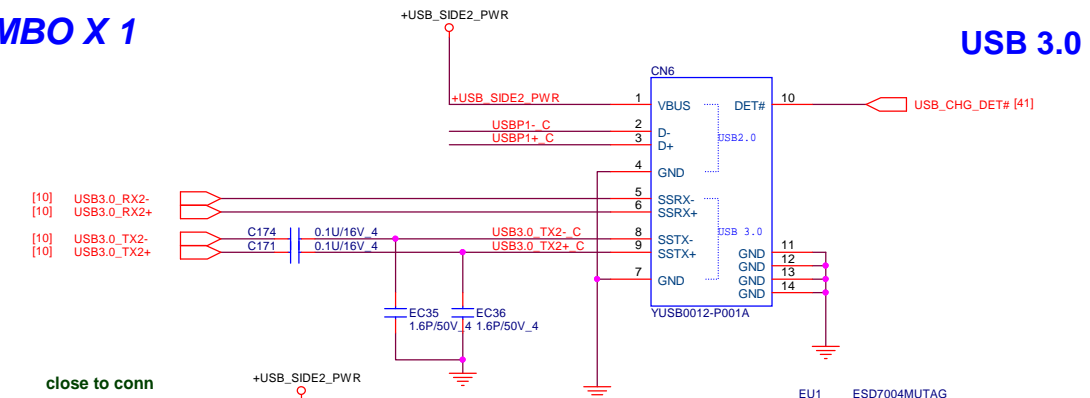
USB Power share

USBP0_BUS_SW_CB0		Mode
Low		DCP, Auto-detect
High		CDP, BC Spec 1.2
OC limitation	R1	mA
	100k ohm	504
	22.1k ohm	2274
	Applied Now	

Current limit = 50500/(R1+0.1)

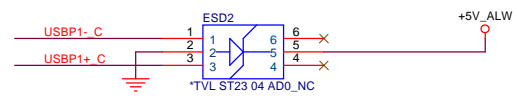
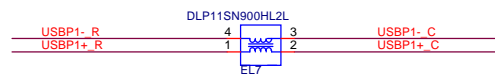


USB3.0/2.0 COMBO X 1



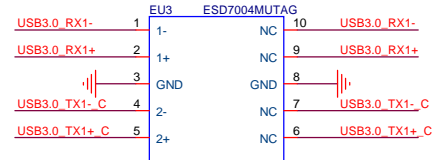
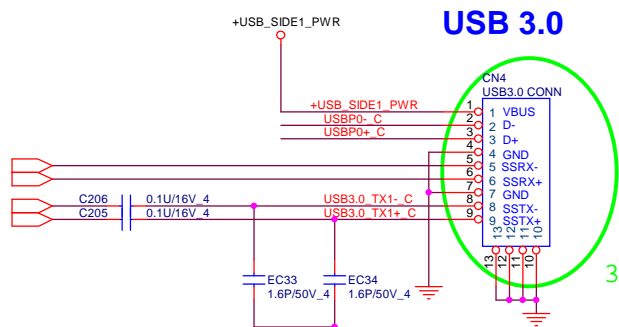
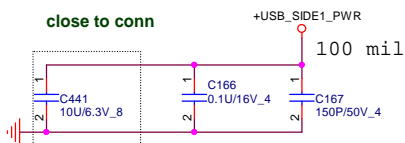
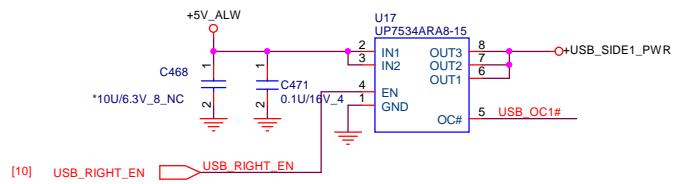
ESD Function

Place ESD diodes as close as USB connector.



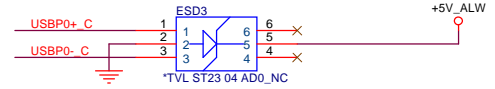
USB3.0/2.0 COMBO

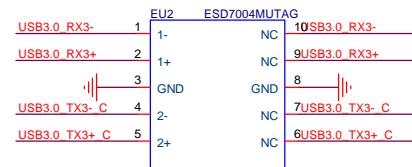
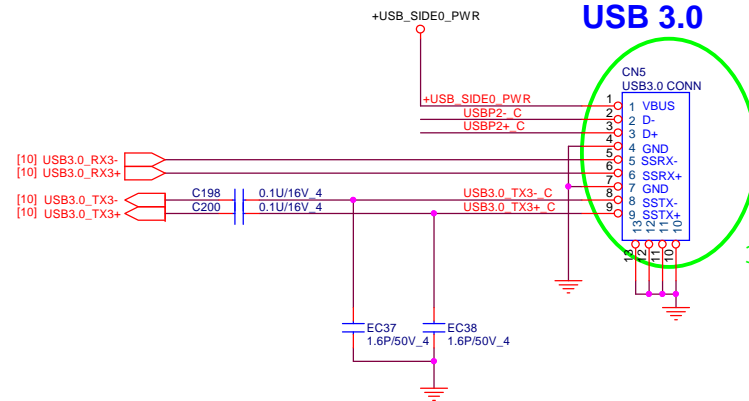
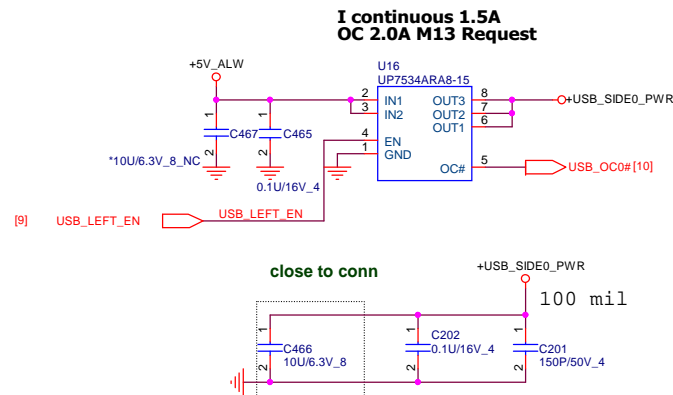
I continuous 1.5A
OC 2.0A M13 Request



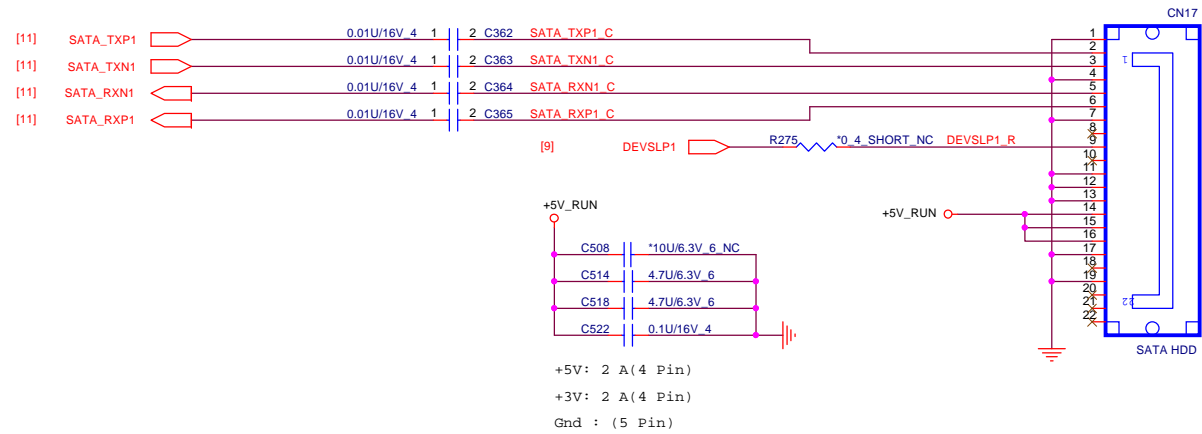
ESD Function

Place ESD diodes as close as USB connector.

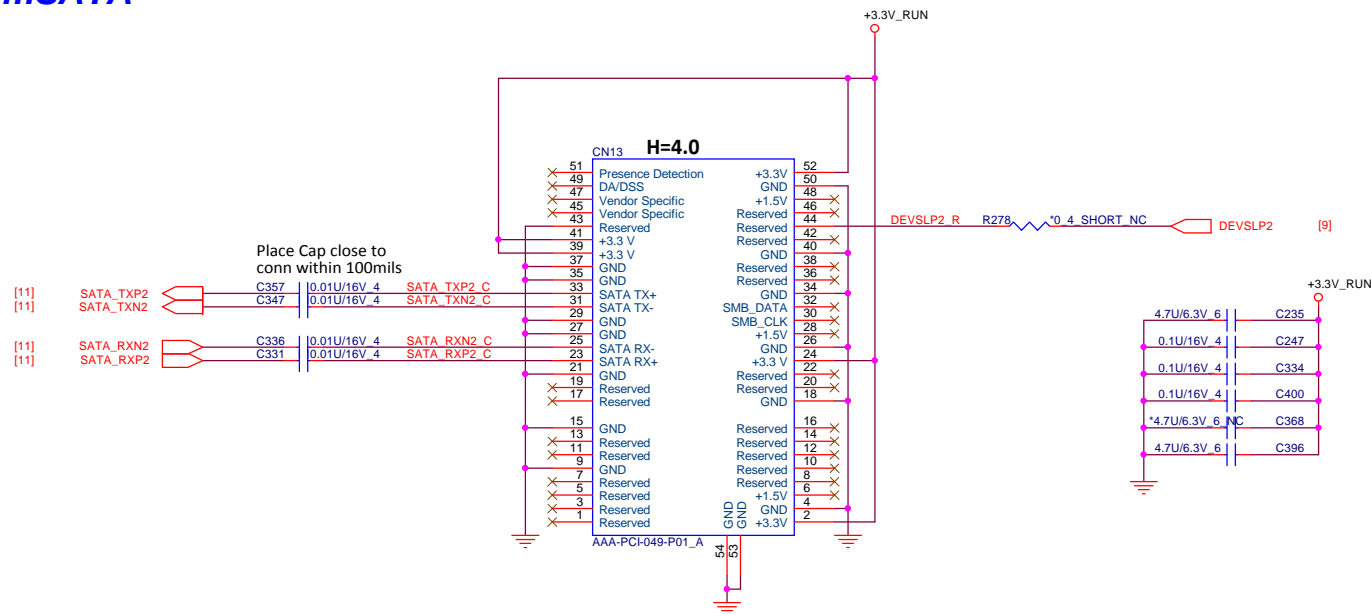




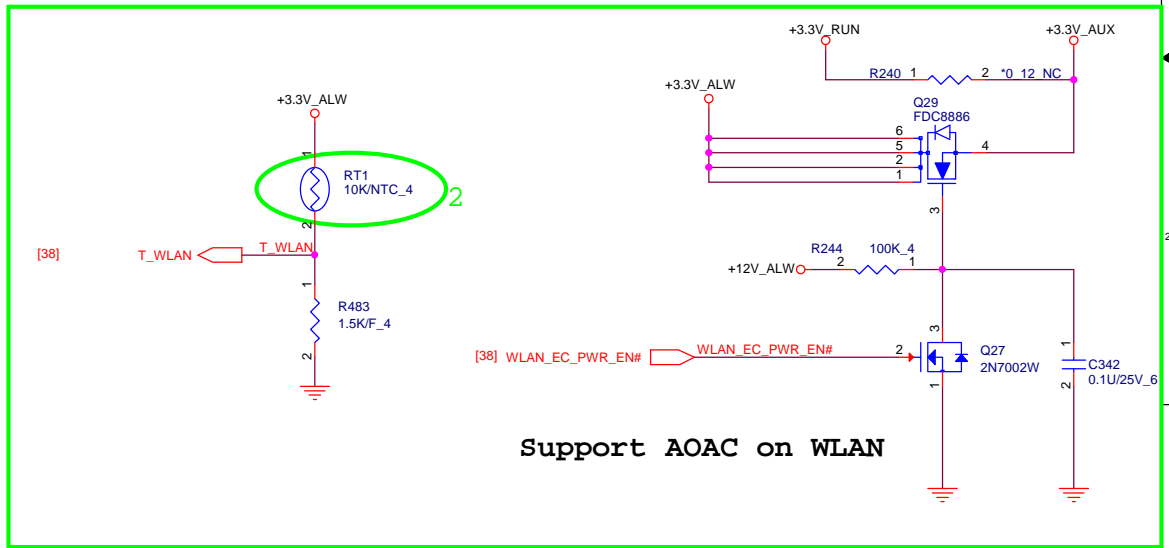
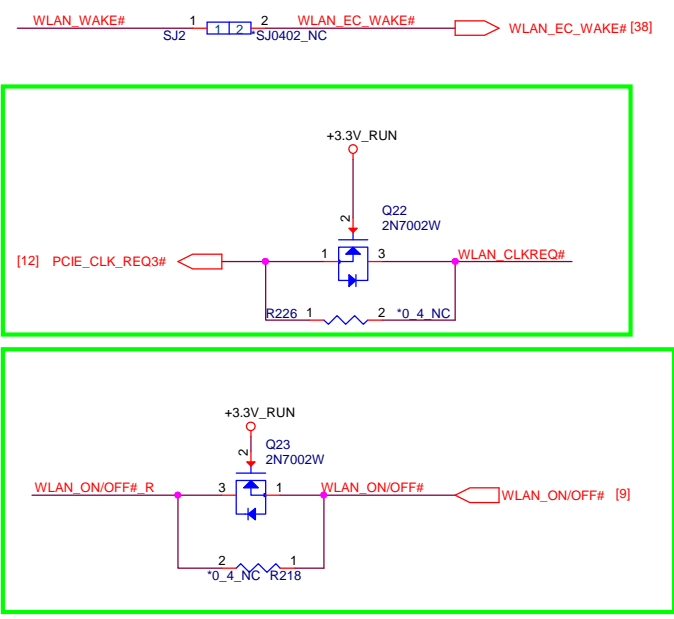
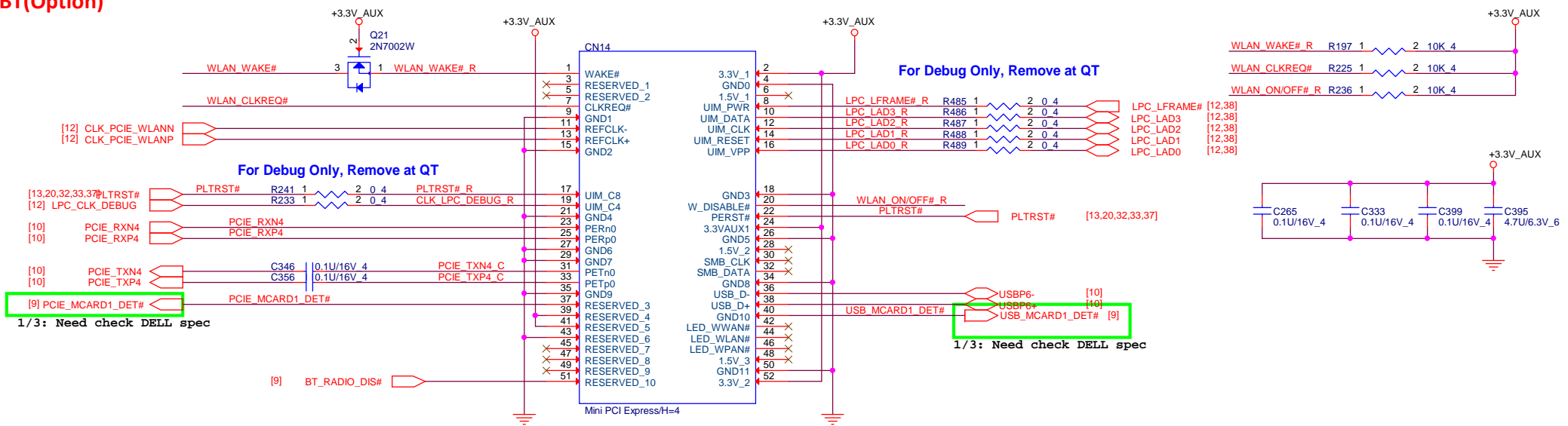
SATA HDD Connector



mSATA

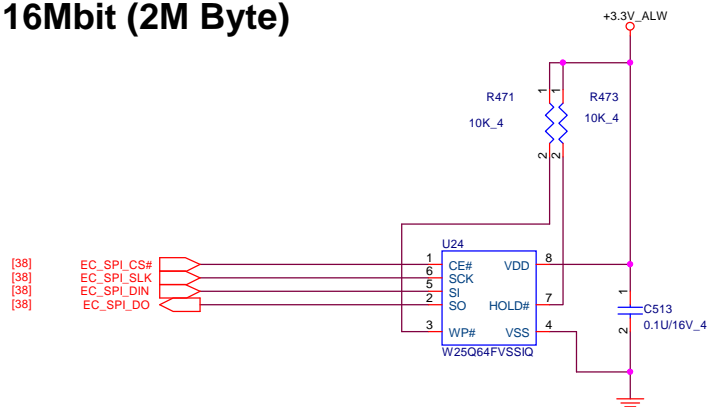


Mini Card WLAN/BT(Optional)

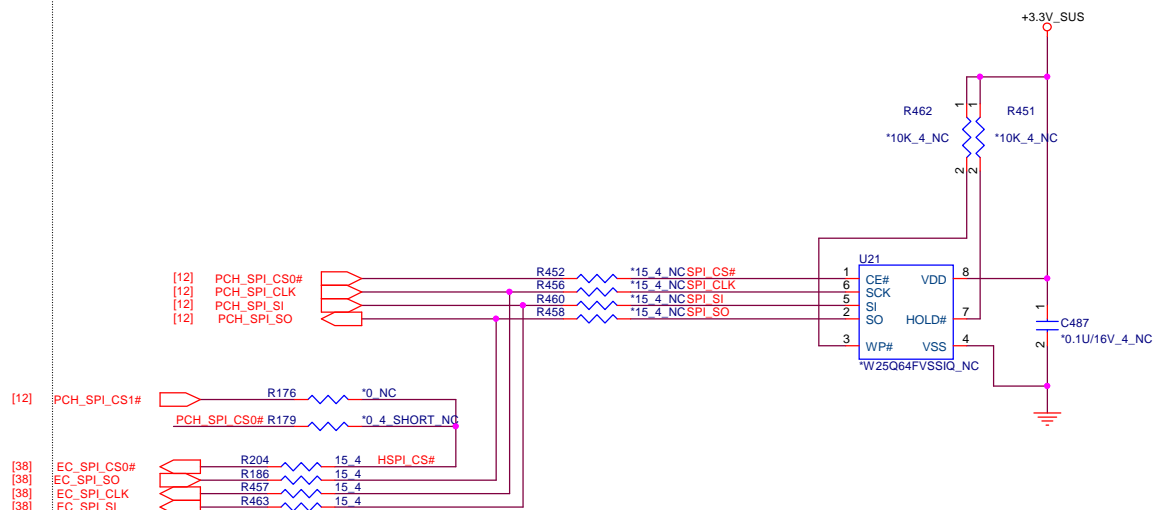




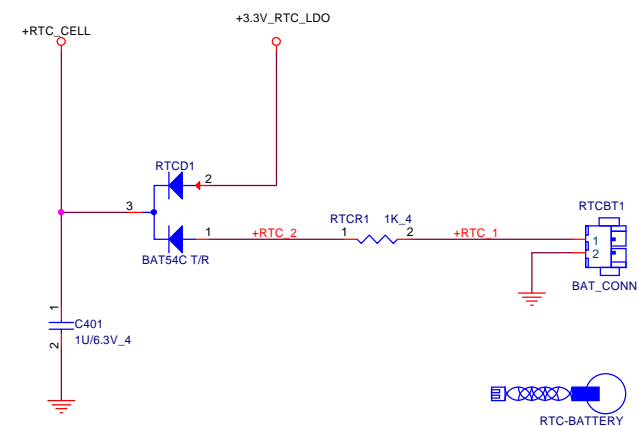
For EC 16Mbit (2M Byte)



For PCH 64Mbit (8M Byte)

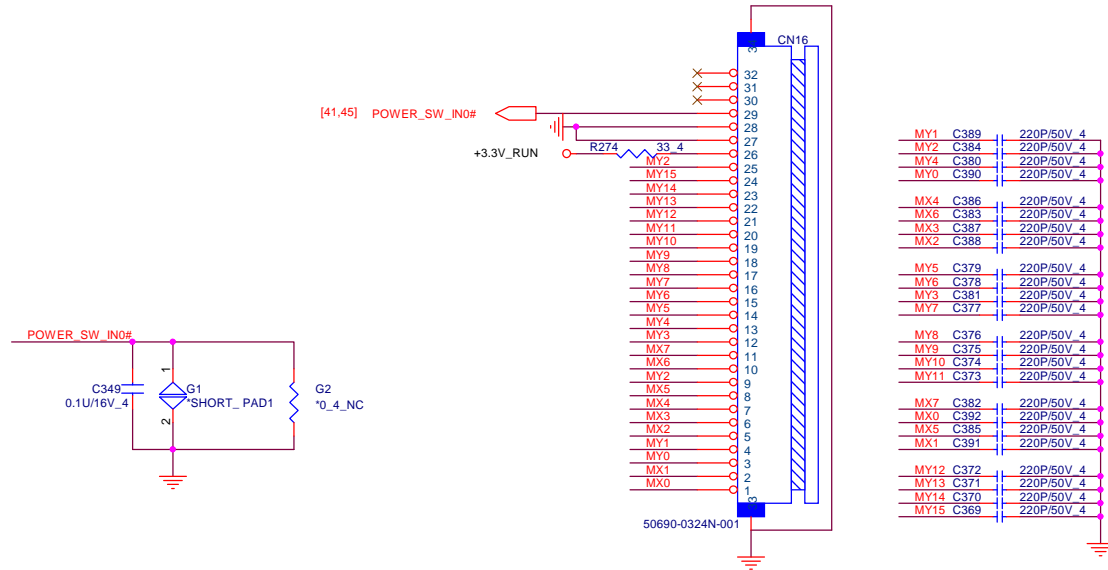


RTC BATTERY

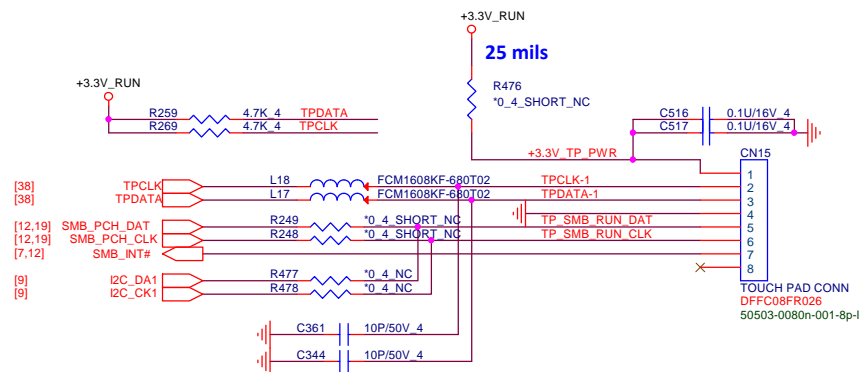


Keyboard Connector

[38] MY[0..15] MY[0..15]
[38] MX[0..7] MX[0..7]



Touch Pad Connector



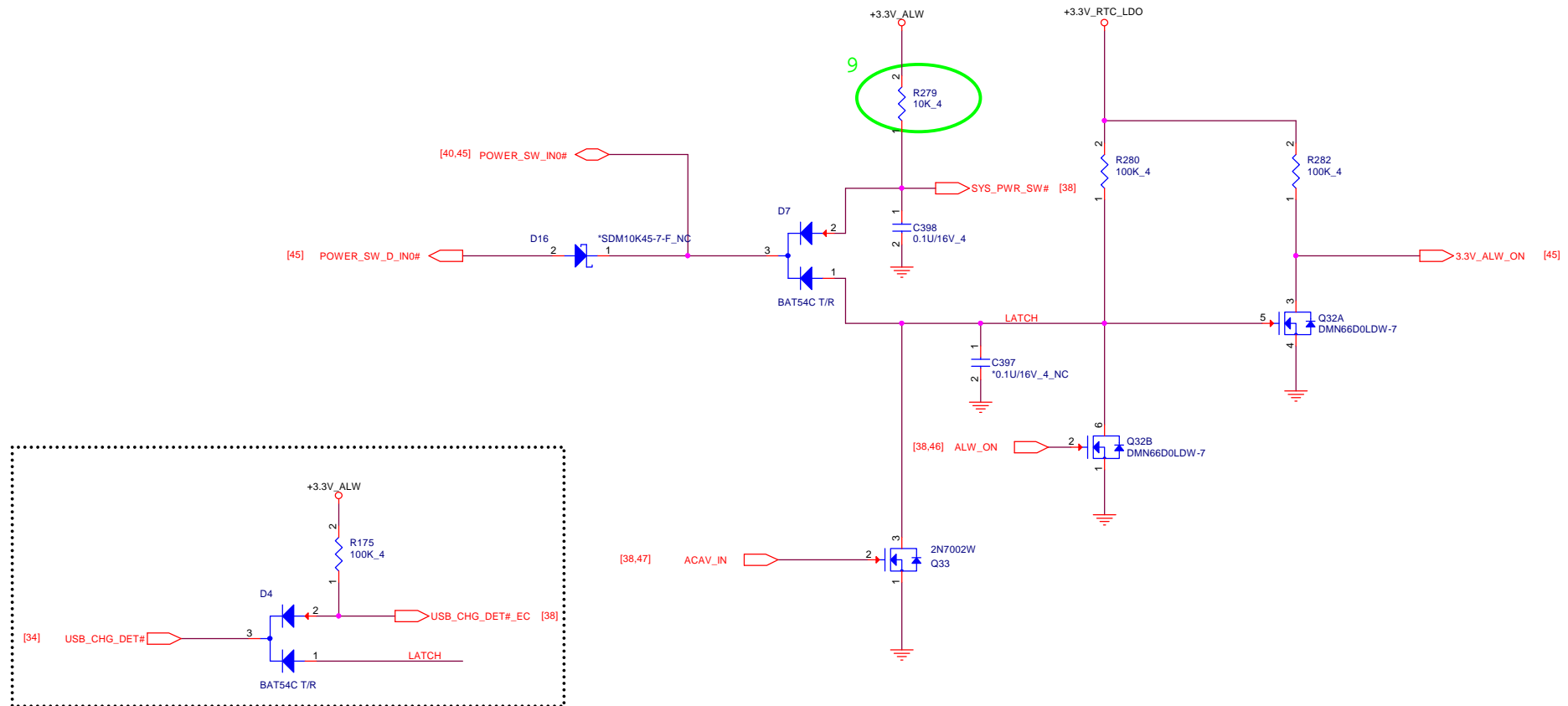
Quanta Computer Inc.

PROJECT : JW8B

KB/CLK Gen/FAN/TP

Size	Document Number	Rev
		A
Date	Monday, July 08, 2013	Sheet 40 of 57

3VALW ON POWER LOGIC



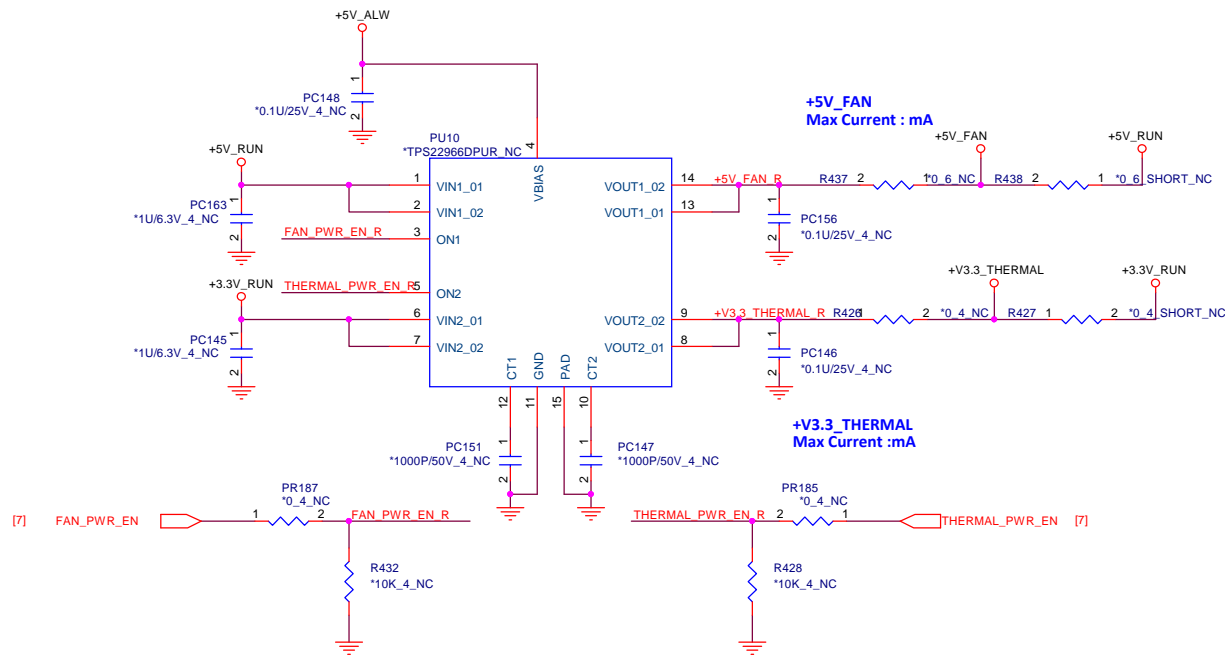
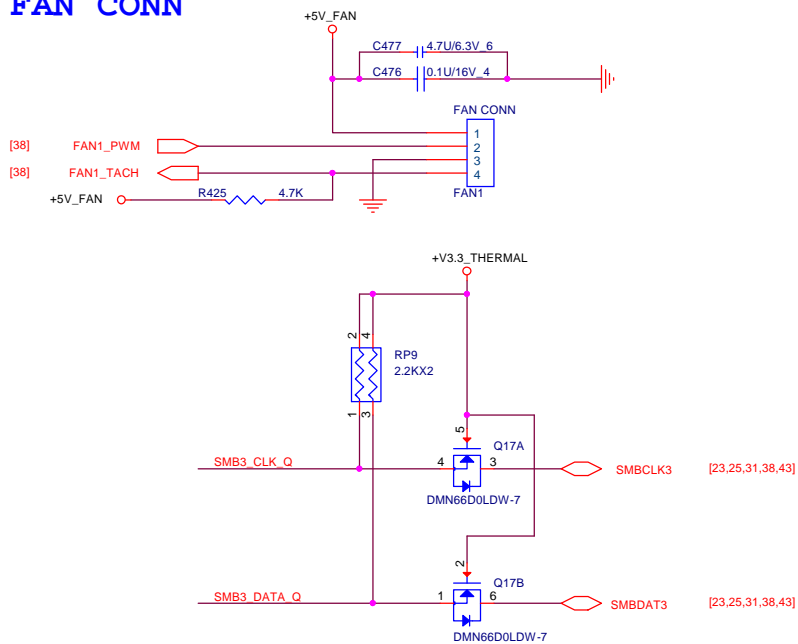
Quanta Computer Inc.

PROJECT : JW8B

3VALW ON POWER LOGIC

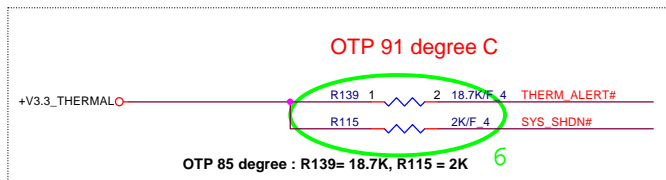
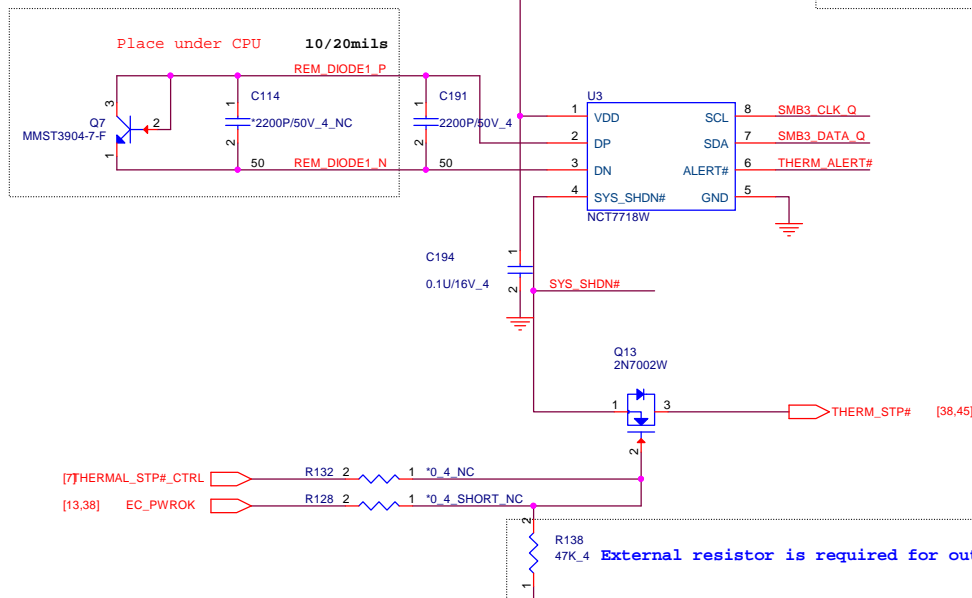
Size	Document Number	Rev
Date: Wednesday, July 17, 2013	Sheet 41 of 57	A

FAN CONN



THERMAL IC

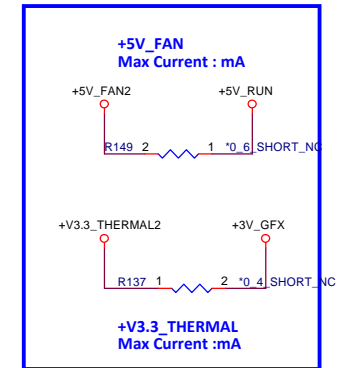
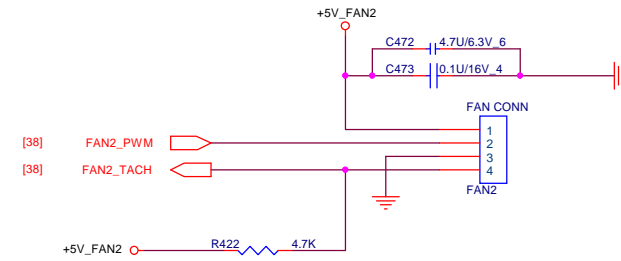
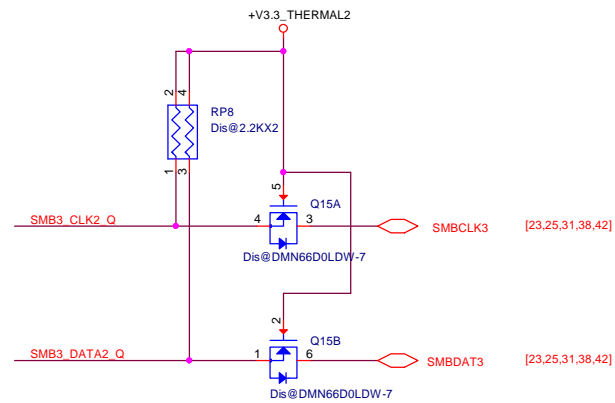
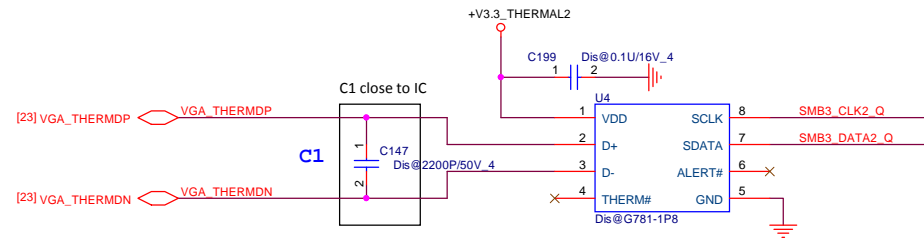
Need closed to CPU



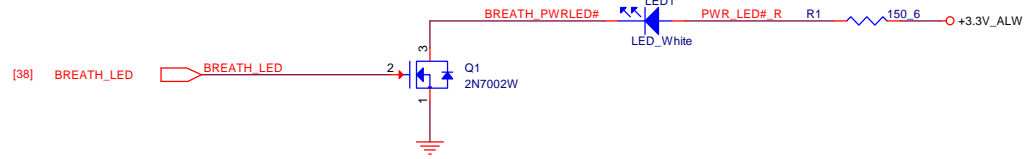
SYS_SHDN#	2K	7.5K	10.5K	14K	18.7K
ALERT#					
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C

FAN CONN

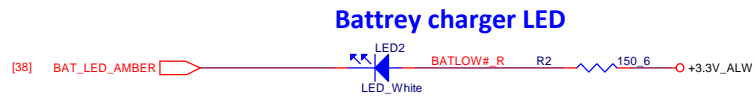
G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).



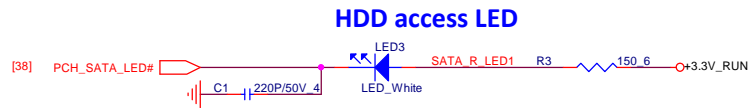
LED Status



System status LED



Battrey charger LED



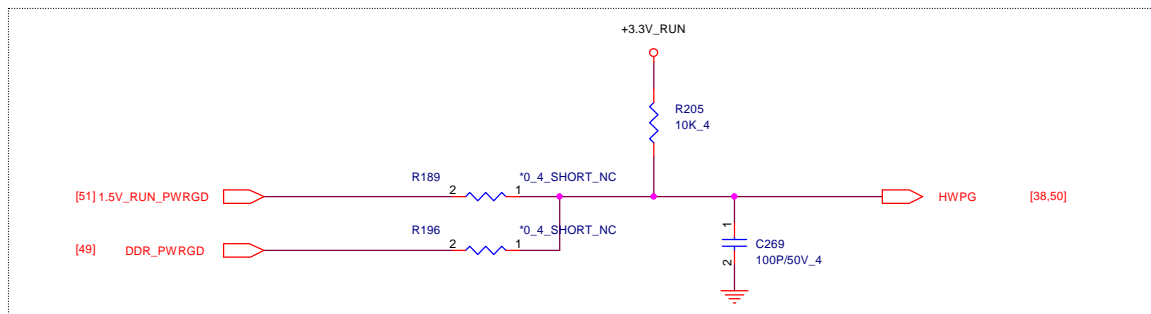
HDD access LED



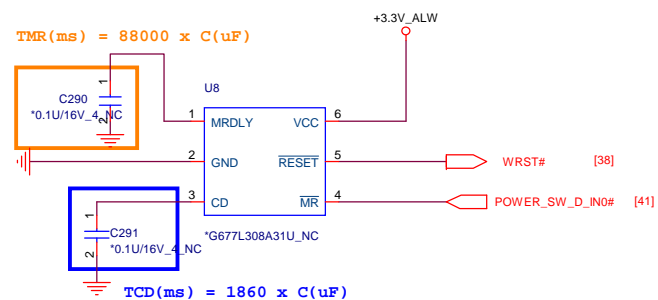
Quanta Computer Inc.

PROJECT : JW8B

Size	Document Number	Rev
	LED	A
Date:	Friday, May 10, 2013	Sheet 44 of 57



HW reset IC



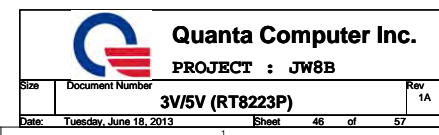
Quanta Computer Inc.

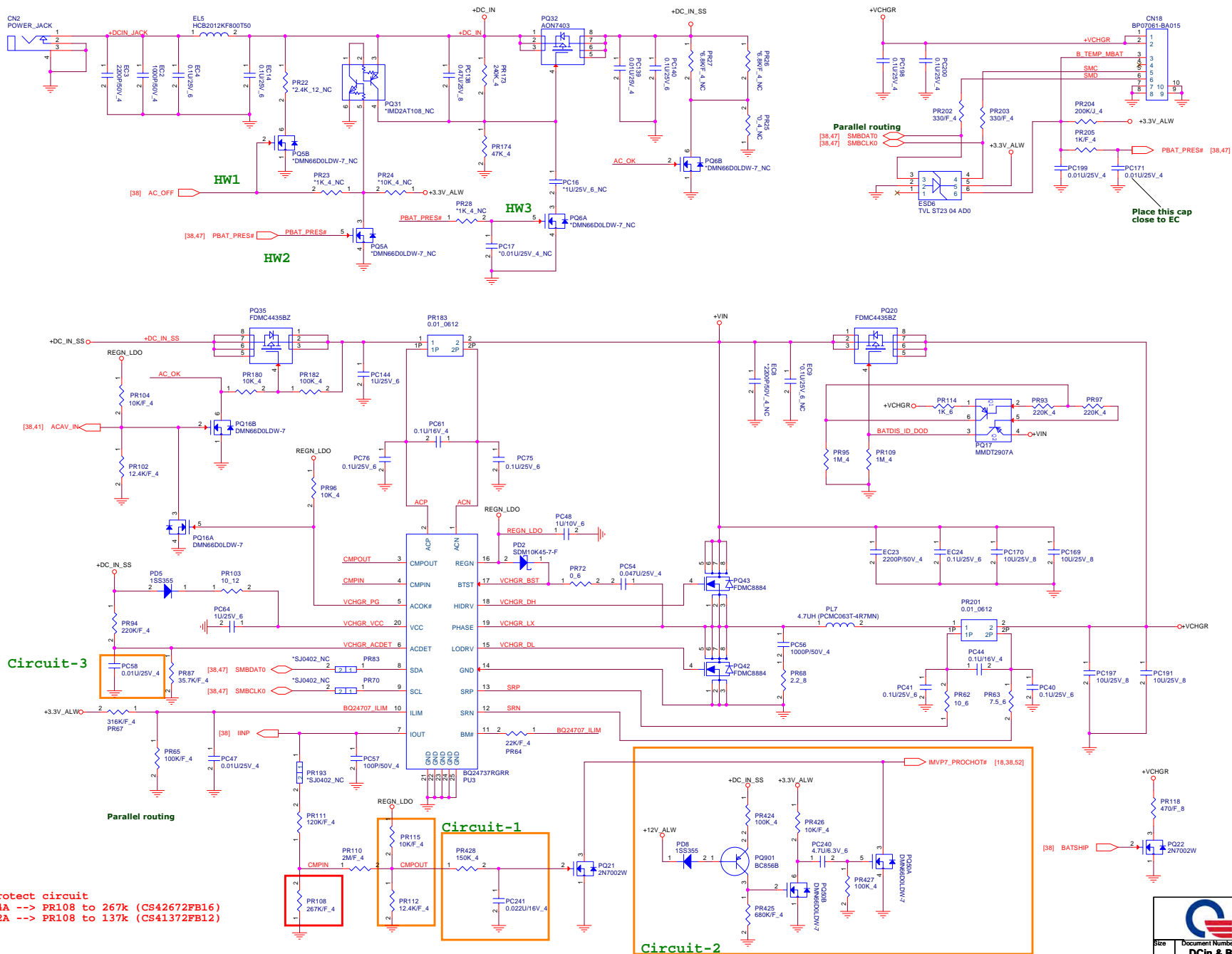
PROJECT : JW8B

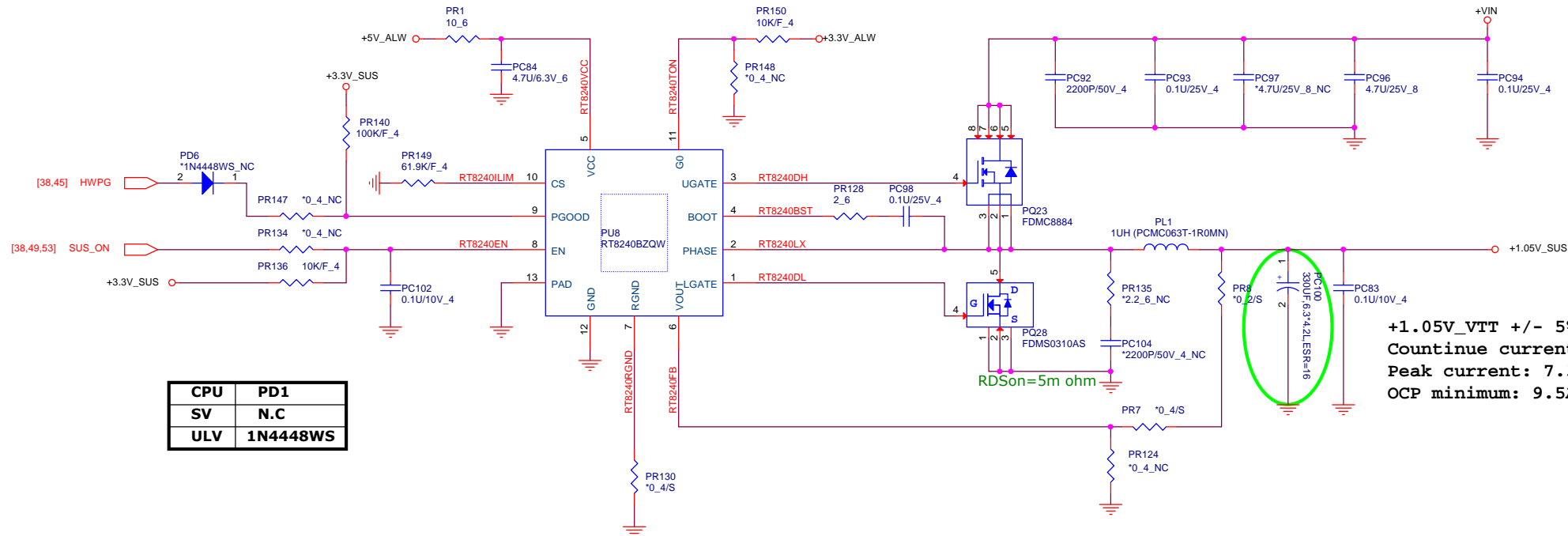
System Reset Circuit

Size	Document Number	Rev
Date: Monday, July 08, 2013	Sheet 45 of 57	A


WWW.AliSaler.Com







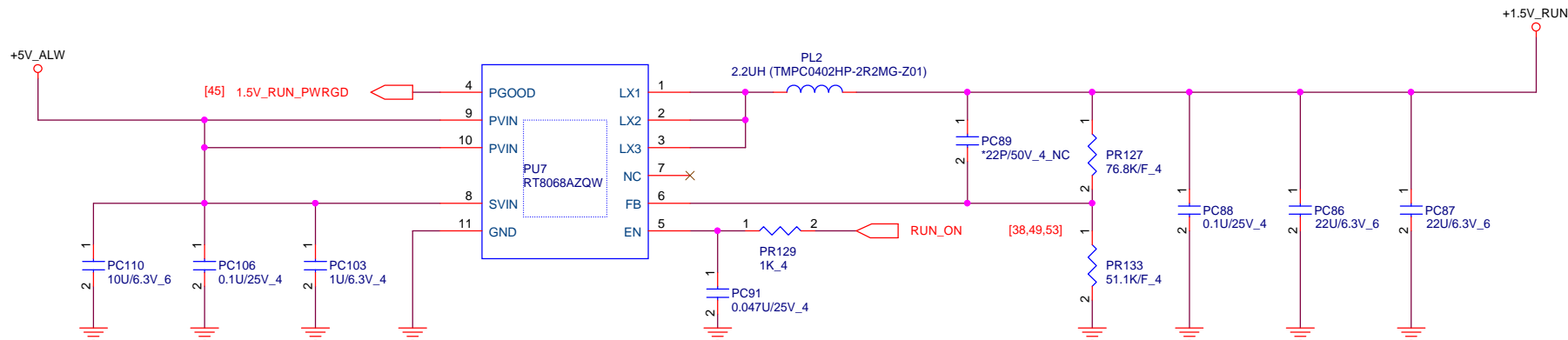
CPU	PD1
SV	N.C
ULV	1N4448WS



Quanta Computer Inc.

PROJECT : JW8B

Size	Document Number	Rev
	+1.05V_SUS (RT8240BZQW)	1A
Date:	Tuesday, July 09, 2013	Sheet 50 of 55



+1.5V_RUN
 1.5 Volt +/- 5%
 Fsw : 1MHz
 TDC : 1A
 Max : 1.5A
 OCP :3A



Quanta Computer Inc.

PROJECT : JW8B

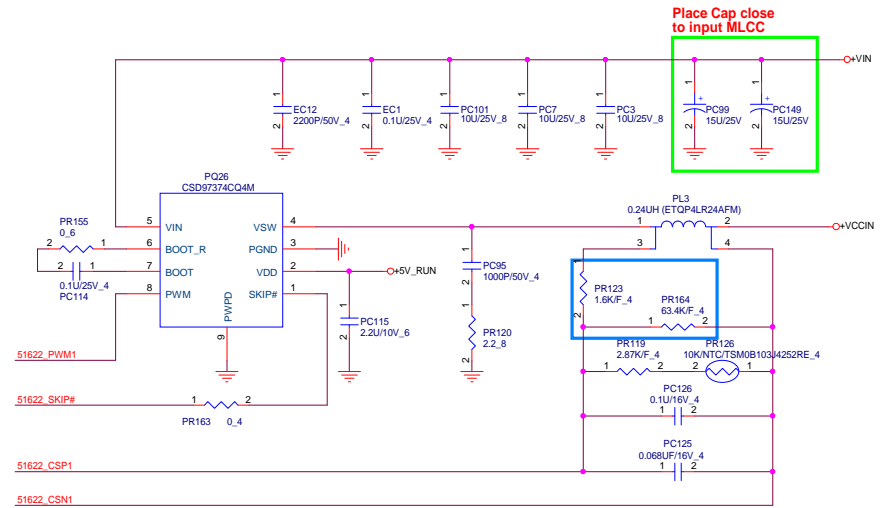
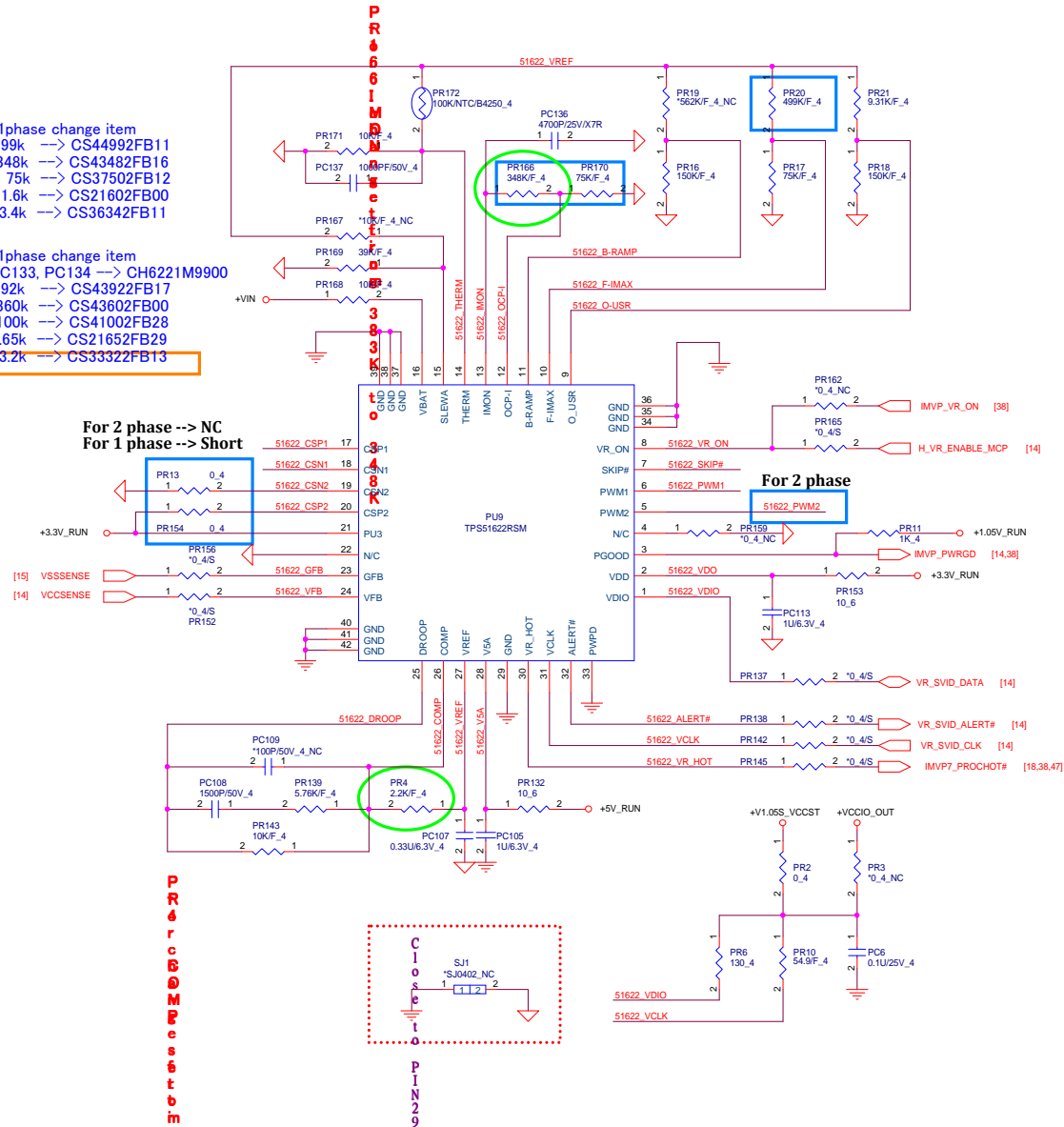
Size	Document Number	Rev
	+1.5V_RUN (RT8068AZQW)	1A

Date: Tuesday, July 09, 2013 Sheet 51 of 57

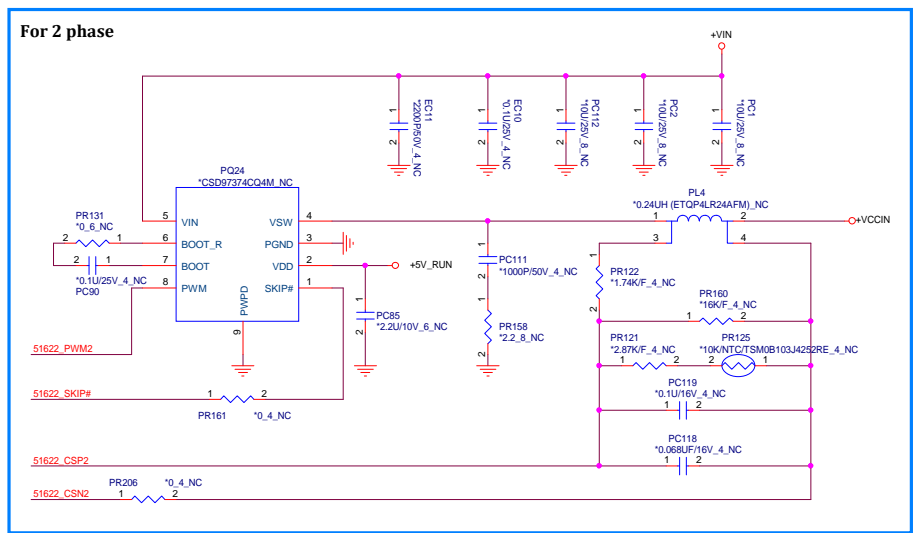
For 15W 1phase change item
 PR20 499k → CS44992FB11
 PR166 348k → CS43482FB16
 PR170 75k → CS37502FB12
 PR123 1.6k → CS21602FB00
 PR164 63.4k → CS36342FB11

For 28W 1phase change item
 PC132, PC133, PC134 → CH6221M9900
 PR20 392k → CS43922FB17
 PR166 360k → CS43602FB00
 PR170 100k → CS41002FB28
 PR123 1.65k → CS21652FB29
 PR164 33.2k → CS33322FB13

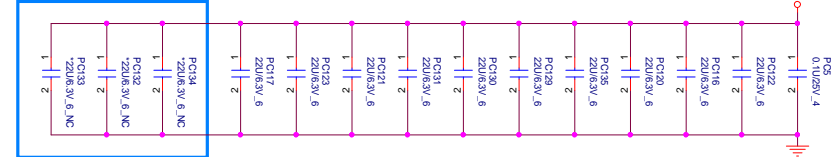
For 2 phase → NC
 For 1 phase → Short

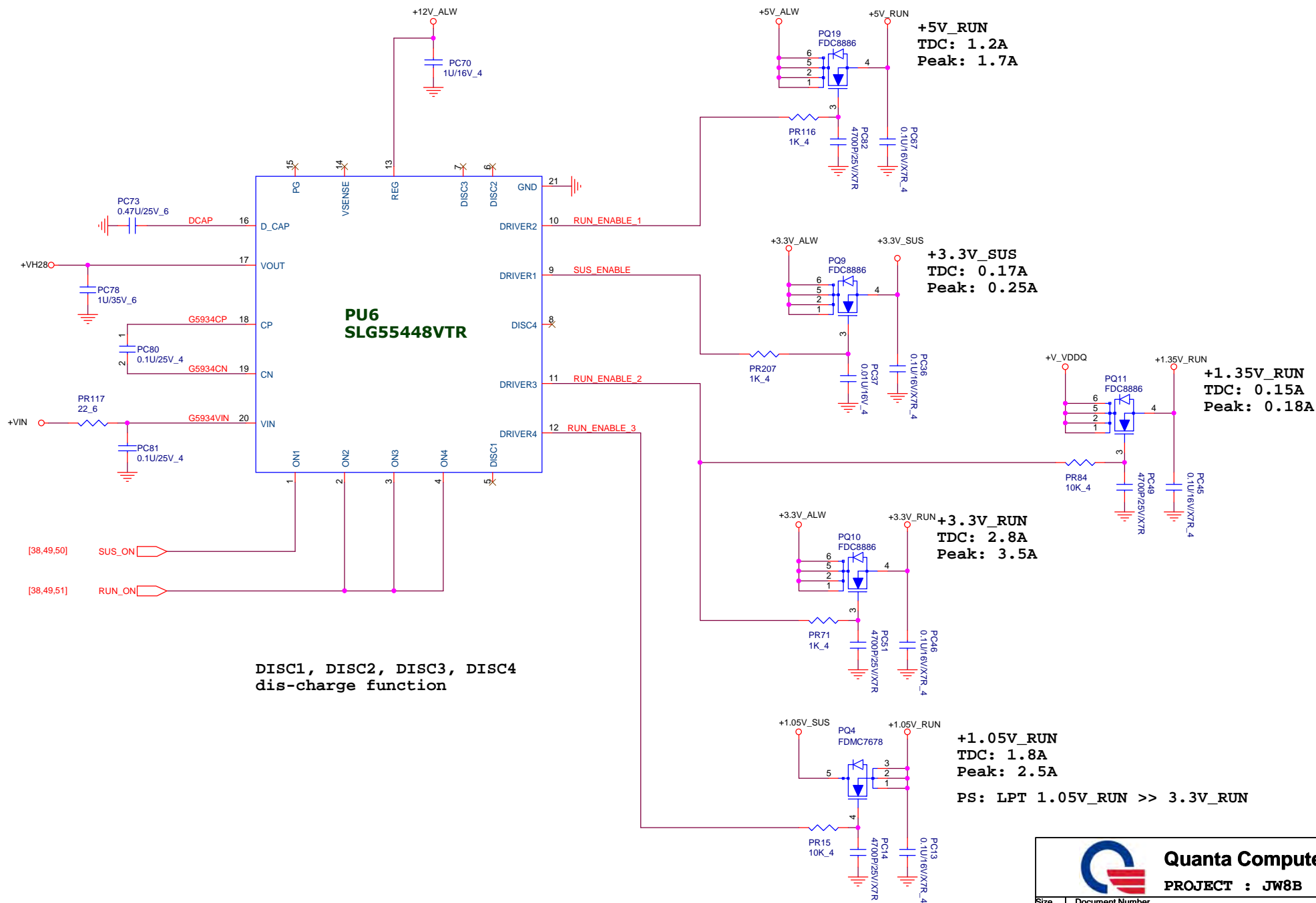


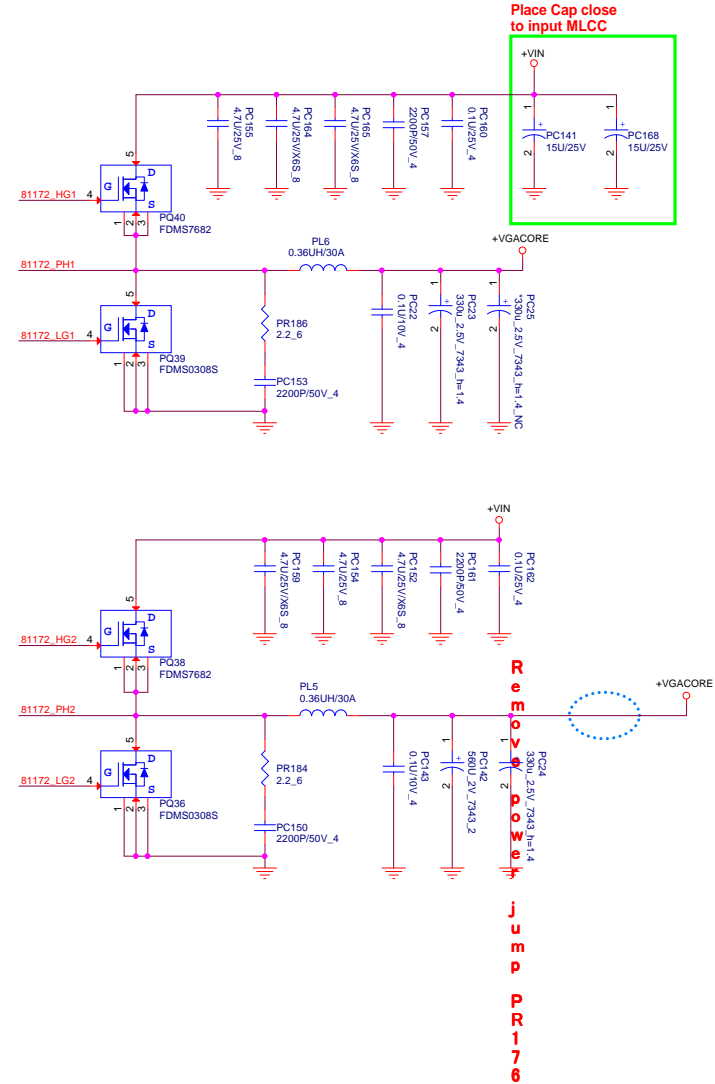
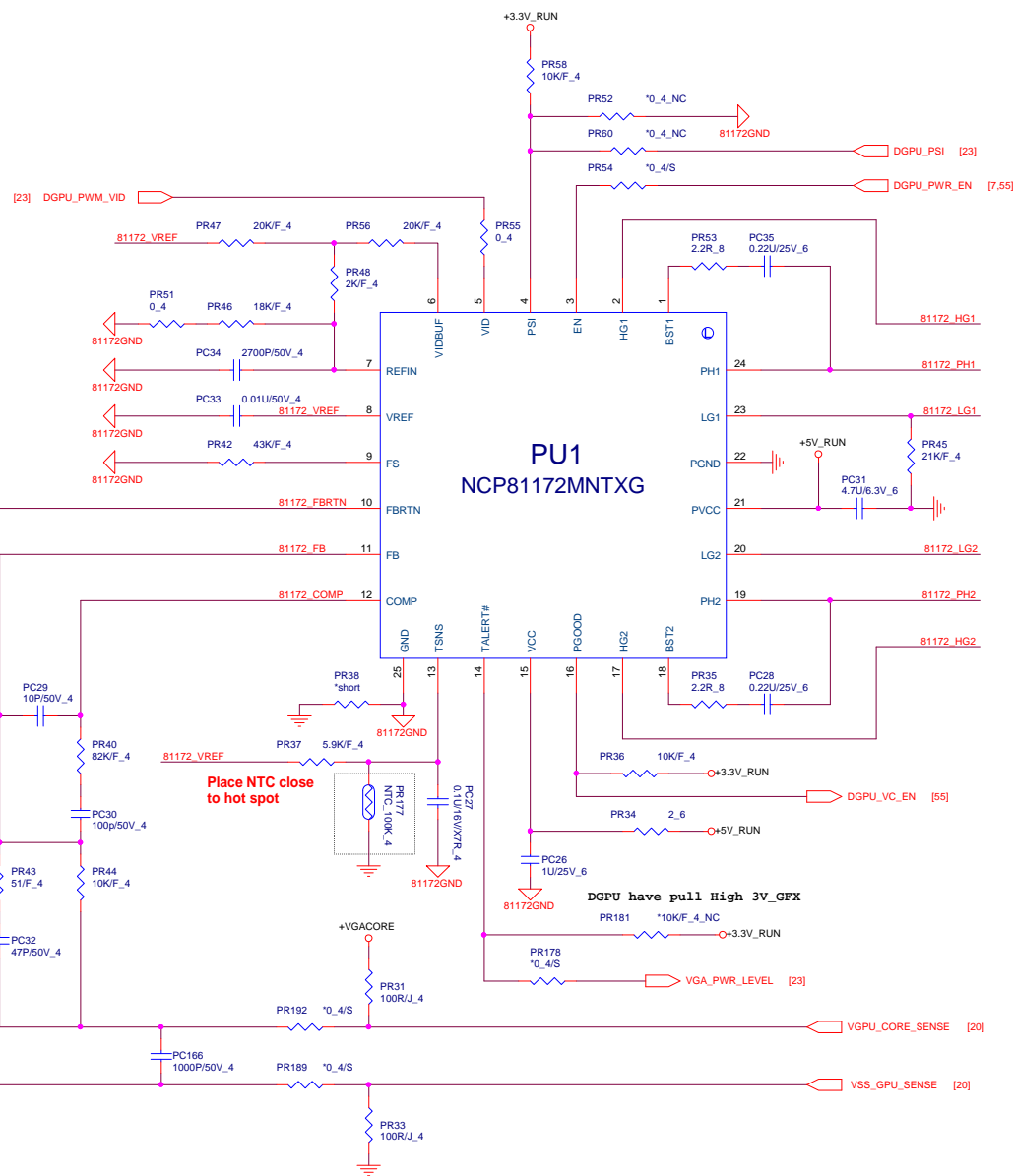
For 2 phase



For ULT 28W









DGPU_VC_EN	H	H	L	L
PS_FB_CLAMP	H	L	H	L
1.5VGFX_OND#	H	H	H	L



+1.05V +/- 3%
Continue current:1.4A
Peak current:2A